Budapest University of Technology and Economics
Faculty of Electrical Engineering and Informatics
Department of Measurements and Information Systems

Gábor Grabicza

MODELLING OF POWER ELECTRONIC SYSTEMS IN ASPECT OF LAYOUT RELATED PARASITIC EFFECTS

Diploma Thesis

INTERNAL ADVISOR

György Orosz

EXTERNAL ADVISOR

András Mersich (Robert Bosch Ltd.)

BUDAPEST, 2018

Table of contents

STUDENT DECLARATION

I, **Gábor Grabicza**, the undersigned, hereby declare that the present MSc thesis work has been prepared by myself and without any unauthorized help or assistance. Only the specified sources (references, tools, etc.) were used. All parts taken from other sources word by word, or after rephrasing but with identical meaning, were unambiguously identified with explicit reference to the sources utilized.

I authorize the Faculty of Electrical Engineering and Informatics of the Budapest University of Technology and Economics to publish the principal data of the thesis work (author's name, title, abstract in English and in Hungarian, year of preparation, supervisor's name, etc.) in a searchable, public, electronic and online database and to publish the full text of the thesis work on internal network of the university (this may include access by authenticated outside users). I declare that the submitted hardcopy of the thesis work and its electronic version are identical.

Full text of the thesis work classified upon the decision of the Dean will be published after a period of three years.

Budapest, 23 May 2018

...…….
Gábor Grabicza

Összefoglaló

Teljesítményelektronikai rendszerek tervezése során kiemelkedő szerep jut a parazita hatások analízisének. Az analízis nem csak az alkatrészek gyártástechnológiájából fakadó parazita hatásokat foglalja magába, hanem kiterjed a topológia, a vezetékezés, az alkatrészek elhelyezéséből származó paraméterekre is. Ezen parazita hatások együttese alapvetően meghatározza az áramkörök teljesítményveszteségeit – melyek a parazita ellenállásokkal állnak összefüggésben – illetve a lejátszódó kapcsolási folyamatokat.

A kapcsolási idők csökkentésével a kapcsolási veszteségek csökkenthetők, ugyanakkor alsó korlátot nyújtanak a járulékosan a rendszerbe kerülő induktivitások. A kapcsolások pillanatában keletkező indukált feszültségek csúcsértékei ugyanis nem léphetik át az alkatrészekre jellemző kritikus értékeket, mivel ez azok meghibásodásához vezethet. A teljesítményelektronikai áramkörökben folyó nagy áramok megszakításakor tehát minden esetben figyelembe kell venni a parazita hatások által okozott indukciós jelenségeket.

Dolgozatomban annak lehetőségeivel foglalkozom, hogy a tervezési folyamat részeként hogyan lehet kifejezetten a topológiából fakadó parazitahatásokat elemezni. A munka szerves részét képezte a végeselem-módszert használó ANSYS Q3D Extractor szimulációs szoftver használatának elsajátítása is, mivel, mint azt vizsgálataim is alátámasztják, ennek segítségével lehetséges a parazita hatások legvalóságosabb modellezése.

Demonstrációs példaként egy klasszikus félhíd-topológiát választottam, melynek tervezése egyszerű, ugyanakkor maga az áramkör reprezentatív, hiszen a kapcsolási jelenségek behatóan vizsgálhatók segítségével. A félhíd áramkör három különböző topológiával valósult meg, nyomtatott áramköri lapon.

Végezetül a parazita analízis különböző módszerei által szolgáltatott eredményeket összevetettem a mérés közben megfigyelt, tényleges működés során lejátszódó jelenségek megfelelő paramétereivel. Munkám kimenete egy, a későbbiekben is jól használható parazitaanalízis-módszertan, melynek fő alappillére a végeselemes mezőszimuláció.

Abstract

Parasitic analysis has a significant role in designing power electronics systems. The analysis does not only contain the derivation of parasitic effects related to the manufacturing technology of components, but also the layout related parameters. The collection of these parasitic effects fundamentally determine the power dissipation – that is linked with the parasitic resistance – and the switching processes of the circuits.

The switching losses can be reduced by reducing the switching times, but the reduction is limited by the parasitic inductances appearing in the system. The induced voltage spikes appearing in the moments of switching due to them are not allowed to exceed the critical characteristic values of the components, otherwise component damage is imminent. When breaking high currents in power electronics circuits, the induction caused by the parasitic effects always has to be considered.

In this diploma thesis, as part of a design process, I overview the applicable methods for parasitic analysis. I focus on the layout related parasitic effects. I also focused on getting experience in use of ANSYS Q3D Extractor finite element software, because according to my assessment, it provides the most realistic modelling of parasitic effects.

I introduce the methods through the example of a classic half-bridge topology. This circuit is simple to design, but is also representative, because a typical switching procedure can be observed through it. The half-bridge circuit is realized with three different topologies, on printed circuit boards.

Finally, I compared the results of parasitic analysis based on different methods with the behavior of real operation. The output of my work is a methodology of parasitic analysis based on finite element field simulation, that can be used in future projects.

Commonly used abbreviations

DC: Direct current

AC: Alternating current

MOSFET: Metal-oxide semiconductor field-effect transistor

HS: High-side

LS: Low-side

IC: Integrated circuit

PCB: Printed circuit board

LTCC: Low temperature co-fired ceramic

HTCC: High temperature co-fired ceramic

DBC: Direct bonded copper

G-S: Gate-source (voltage)

D-S: Drain-source (voltage)

SOIC: Small outline integrated circuit

Ecap: Electrolytic capacitor

THT: Through-hole technology

FEM: Finite element method

FEA: Finite element analysis

PDE: Partial differential equation

2D: Two-dimensional (geometry model)

3D: Three-dimensional (geometry model)

PDE: Partial differential equation

FVM: Finite volume method

ESR: Equivalent series resistance

ESL: Equivalent series inductance

1 Introduction

Parasitic analysis is important in every field of electronics. Construction of electrical systems always has to contain the analysis of non-ideal effects related to the components, the environment, the layout, etc. There are commonly used methods to execute the parasitic analysis. Some of these are based on rules of thumb, estimations and approximations. Nowadays the numeric methods such as finite element simulations seem to be the most accurate ones. Some measurement methods are available after manufacturing, to validate the preliminary estimations.

In this area of electronics, nothing can be completely exact. The models can always be refined, and even more and more effects can be considered. However, usually it is not a requirement to model all the possible effects. We are usually interested in the operation of the total system. Observation of every effect coming forward is not a goal when the product is already in use. This kind of analysis is only applicable during design phase. Proper planning ensures that the user does not have to be concerned about the parasitic effects.

In power electronics, the power dissipation is the most critical point of the system. Manufacturing technologies evolve on a daily basis; undesired effects are continuously reduced, but still achieving. This is why for example the layout related parasitic effects have to be considered. In this diploma thesis, I analyze some possible methods to model these effects. Let's see, why is it important to deal with them.

Resistance of the elements of the layout (such as conductive paths, wires, lands, pins and pads, components' leads, etc.) essentially influence power dissipation, according to Equation 1-1. These parameters cause ohmic losses.

$$P_{diss} = I_{RMS}^2 \cdot R$$

Equation 1-1: Power dissipation

These resistances have to be minimized, because of not only the unwanted dissipation losses, but also the self-heating of the system, which can damage the components, the layout, the housing, etc.

Dissipation is also linked to switching processes. Due to the switching transients, so-called switching losses appear. The longer the switching procedure takes, the higher is the power dissipation due to it. According to it, the goal is to minimize the switching times.

On the other hand, inductances of the conductive paths cause induced voltage spikes in the moments of switching, according to Equation 1-2. The faster the switching is (and so the shorter the switching times are), the higher the amplitude of the induced voltages are.

$$V_{ind} = -L \cdot \frac{dI}{dt}$$

Equation 1-2: Induced voltage

This effect is critical in aspect of electromagnetic compatibility (EMC). Disturbing other systems has to be avoided according to standards. Another problem is that the components (for example semiconductors) have critical voltages, which can not be exceeded, in fear of damaging them.

As a result, switching times are limited from two sides. EMC standards and critical parameters provide a lower limit and switching losses determine the upper. The optimal values have to be found during the design process.

In this diploma thesis, I would like to introduce a design procedure augmented by parasitic analysis. I focus only on layout related parasitic effects. I demonstrate the method of parasitic analysis through the example of a half-bridge circuit from the planning to the testing of the circuit. A half-bridge is a simple and easy to understand electronics module with all the interesting switching characteristics. It is a simplified but representative model of all power electronics.

The thesis begins with a short power electronics overview (Chapter 2). It summarizes the most important properties of bridge circuits (H-bridges and half-bridges).

Chapter 3 contains the steps and considerations of the design process. The operation of the half-bridge circuit is also demonstrated in this chapter. The goal was to design several (in this case three) different layouts based on the same circuit schematic, and analyze the difference between the parasitic effects related to the different layouts. Testability had to be considered during the design of the layouts. This means that the three layouts had to show considerable difference for one to be able to compare them, but only in the layout related effects. I also had to design proper contact points for the measurement instruments.

Chapter 4 is about the theory of parasitic analysis. In this chapter, I summarize the possibilities of modelling parasitic effects. The simplest methods are rules of thumb and estimations. These methods are often used, but have limits that are (incorrectly) not always considered. A more sophisticated method is using a field simulation software

based on finite element method (FEM). In this project, I used the Q3D Parasitic Extractor software module of ANSYS Electromagnetics. One of the goals of this project was to get experience in the application of this software, because – as it is being shown – it is the most appropriate method to model the layout related parasitic effects. I introduce it in Chapter 4.3. At the end of Chapter 4, I introduce some measurement techniques to determine parasitic effects. Testing them was not part of my work, so it is only a theoretical overview.

I experimented with the methods mentioned (Chapter 5). According to Chapter 6, I used the derived data as input for simulations, and as it can be seen in Chapter 8, I compared the simulation results with the measured characteristics (presented in Chapter 7) to find the most appropriate method(s). Finally, as the output of my work, an applicable methodology was born, that is appropriate to use in the future with some additional considerations.

2 Power electronics basics

In this chapter, I am going to provide a short power electronics summary. I would like to overview the properties of bridge circuits, especially half-bridge circuits. Here I would like to highlight that this summary is limited only to those properties of the circuits, components etc., that are relevant in aspect of this diploma thesis. I assume a basic knowledge in theory of semiconductors.

2.1 Bridge circuits in power electronics [1] [2]

A bridge circuit is a special topology in electronics. These circuits have two or more main branches that are connected by other branches at the same intermediate points of them. There are bridge circuits for measurement applications too (for example the Wheatstone-bridge), but I focus on driving specific bridges. In these circuits, the connecting branches are coils of a motor. These are used for example in power inverters and converters. In power electronics, the most widespread application of them is motor controllers.

2.1.1 H-bridges

The most frequently used bridge circuit is the H-bridge, which is shown in Figure 2-1.

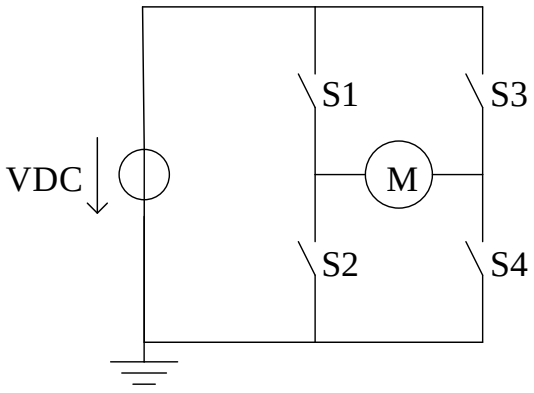


Figure 2-1: H-bridge

It contains four switches (S1 and S2 in the first branch, and S3 and S4 in the second one) and a DC voltage source that provides the supply current. The load, for example a coil of a motor (M), is connected to the center point of the branches. There are

two different states of the H-bridge. Exactly one switch is on and exactly one switch is off at the same time in both branches. If both switches would be on in the same branch, the source would be shorted, which can cause the damage of components. This phenomenon is often mentioned as cross conduction or shoot through.

When S1 and S4 are closed (and S2 and S3 are opened), the current flows through the load in the direction from the first branch to the second one.

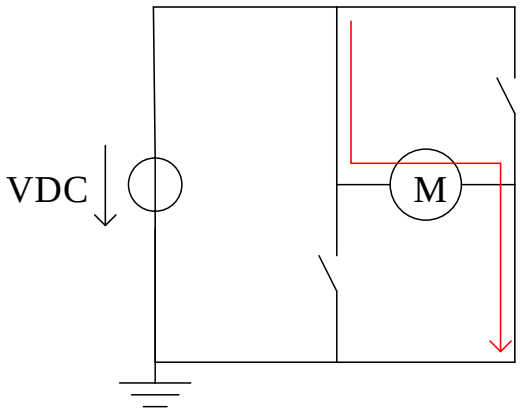


Figure 2-2: H-bridge operation, state 1

In the other state, S2 and S3 are closed (and S1 and S4 are opened), and the current flows in the direction from the second branch to the first one.

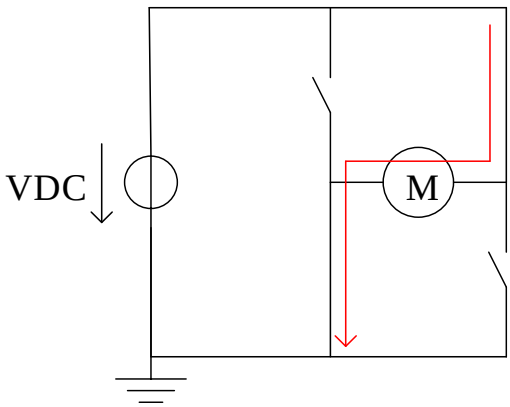


Figure 2-3: H-bridge operation, state 2

When the state changes, the direction of the current flow through the connecting branch also changes, and it makes the motor run forwards and backwards.

The switches of the bridge circuit need a controlling logic that guarantees the proper operation. It has to ensure that only one switch is on, and only one is off in one branch at the same time. When nonetheless there is a short circuit because of two closed switches at the same time, it is expected that the controlling logic can handle the situation

(for example by switching off the supply voltage immediately). It also has to ensure the expected switching times.

With this concept, three- or more-phase motors can also be controlled. The number of the controlled phases depends on the number of the branches.

2.1.2 Switches in bridge circuits

The switches of the bridge circuits can be realized with different devices. In the first applications electromechanical switches, relays were used. The disadvantages of these components are their big size, slow switching ability, the necessity of high driving voltage and ageing. Mechanical parts can often cause problems in electrical circuits.

It is common to use a pair of a PNP and an NPN bipolar junction transistor (BJT) in the same branch. The sign of the control voltages of them is opposite, that is, why this construction is practical in aspect of controlling, because the required voltages can be produced easily. Using a pair of N- and P-channel field effect transistors (FETs) is also a common solution. Its advantage is that the FETs' channel resistance is lower than the BJTs', so the ohmic dissipation can be decreased, and additionally, these components are faster, too, and that reduces the switching losses.

The most efficient realization of the switches is using N-channel metal-oxide semiconductor field-effect transistors (henceforward MOSFETs) as voltage controlled switches. The channel resistance of these devices is smaller than P-channel ones, so the power dissipation can be minimized. In this case, the controlling logic has to consider that the gates of the MOSFETs have to be controlled with positive voltage. This problem can be solved with charge pump or bootstrapping structures (see the latter in 3.2.2).

MOSFETs are commonly used components in electronics. Special groups of these components are applied in power electronics, referred to as power MOSFETs. These components are optimized to conduct large currents periodically, with short witching times. They function as high current switches. I only use N-channel MOSFETs in this project, so henceforward the word 'MOSFET' always means an N-channel one. The circuit symbol of an N-channel MOSFET is shown in Figure 2-4:

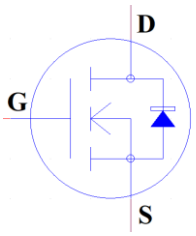


Figure 2-4: N-channel MOSFET circuit symbol

The device's three electrodes are gate (G), drain (D) and source (S). The channel of the MOSFET is between drain and source. The diode between the source and the drain is called intrinsic (or body) diode. It is a parasitic diode that is a side effect during the semiconductor construction. In half-bridge circuits, it is often used for freewheeling (see in Chapter 3.4.2.2). Henceforward, the switches of the bridge circuits are assumed to be N-channel MOSFETs.

The main parameters of a MOSFET can be found in the datasheet provided by the manufacturer. It is important to check the properties before deciding to use a particular device. In this project, I used a MOSFET of type IPB100N04S4-H2 by Infineon. It is an N-channel power MOSFET in TO-263 case (or D2PAK). It has a low channel resistance (2.4 mΩ), which results low voltage drop on the device. Its maximal D-S voltage is 40 V. The device can conduct 100 A continuously, it was enough for my goals. Additionally, this device has an online available PSpice model containing the assumed parasitic effects, that I could use in the simulations.

Figure 2-5: D2PAK (TO-263)

At the operating point I used the device, the dissipation and the thermal operation are not critical, so the analysis of these were not part of my work. I am going to mention these topics, but that is not the main goal.

I would like to disambiguate that when I write that a MOSFET is 'on' or 'opened', it means, that the device conducts current. When it is 'off' or 'closed', it does not conduct. It is not the same at switches: when a switch is on (or closed), it conducts, when it is off or opened), it does not conduct. Although it is unambiguous in English, I think it is useful to note for Hungarian readers (in the Hungarian language, these cases have the opposite meaning, and it often causes misunderstanding).

2.2 Half-bridges

2.2.1 Introduction

One branch of a bridge circuit is often referred to as a half-bridge (or rarely half-H-bridge). In this project, I deal with half-bridge circuits in aspect of transient effects. A simple half-bridge contains two switches, a DC voltage source and a two-pole load. The load can also be for example a coil of a motor, like in H-bridges. As it is shown in Figure 2-6, it can be connected between the phase terminal (the common point of the two switches) and the ground or the battery. One half-bridge can control one phase of a multiphase motor.

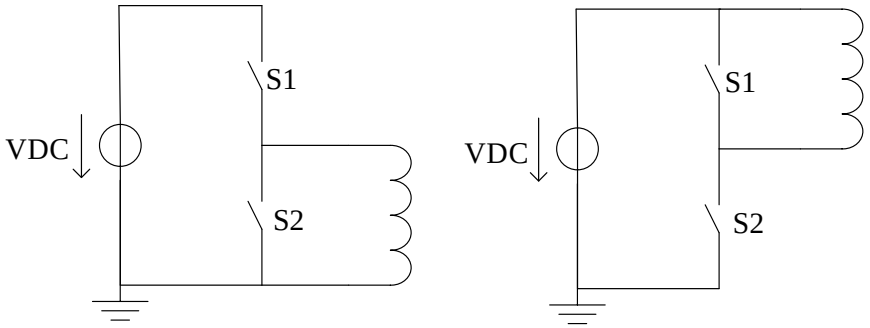


Figure 2-6: Half-bridge topology variants

The half-bridge works like one branch of the H-bridge: one of the switches has to be on and one of them has to be off at the same time. The proper switching is arranged by a controlling logic. Figure 2-7 and Figure 2-8 show the operation when the load is connected between the phase terminal and the ground. In the first state, the current flows through the closed S1 switch and the load:

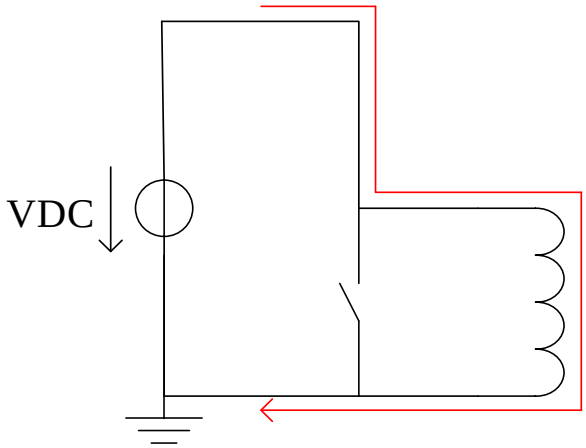


Figure 2-7: Half-bridge operation, state 1

In the second state, S1 is opened and S2 is closed. Assuming ideal components, two different situations are distinguished. If the load is purely resistive (it only has resistance, its impedance is real), zero current flows in the second state, because the circuit of the voltage source is opened, and there are no energy storage elements in the circuit.

If the load has inductance, magnetic field appears due to it. In the second state, its energy starts to dissipate on the resistance of the load. In this case, the current circulates through the closed S2 switch and the load, until the energy becomes zero (or the system steps into the first state again). This effect is called freewheeling, especially active freewheeling, because the S2 switch is controlled. Of course, in real applications there is inductance not only in the load, but in the other components, and the layout' conductive paths, too (that is the main focus of this thesis). It means, that freewheeling always occurs.

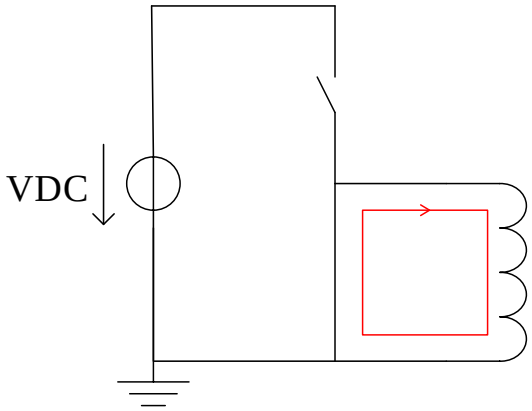


Figure 2-8: Half-bridge operation, state 2 (freewheeling)

Freewheeling also occur, if the S2 switch is replaced with a diode. In the first state, there is negative voltage between the diode's anode and cathode, the current is zero (assume that the leakage current can be neglected). In the second state, the voltage between the diode's anode and cathode is positive, so current flows through it. Its advantage is that controlling is not needed, that is why this phenomenon is called passive freewheeling.

When the switch is realized by a MOSFET, active and passive freewheeling is also possible due to the body diode. If the MOSFET realizing S2 is not switched on in the second state (only the MOSFET realizing S1 is switched on and off in the process), the freewheeling is passive, the current can only flow through the intrinsic diode. If the MOSFET realizing S2 is also switched on and off with proper timing, the freewheeling is active. In this case, the current flows through the MOSFET's channel and the diode parallel with it. It means that the effective resistance is much lower (due to the low

channel resistance, which is connected parallel with the diode's higher dynamic resistance), and the voltage drop on it is also lower. That is, why active freewheeling is advantageous, because resistance is proportional to power dissipation according to Equation 1-1, so lower impedance results in lower dissipation. Its disadvantage is the required controlling of the MOSFET realizing switch S2.

The process is the similar, when the load is connected between the phase terminal and the battery voltage. In this case, S2 conducts the current in the first state, and in the second state the current circulates through S1 and the load.

In the above discussion, several secondary effects were neglected. In real applications, the parasitic effects of the wires, the load, the connectors, the switches etc. have to be considered. In the next chapters, I am extending the limits of this model.

2.2.2 General operation of half-bridge circuits

2.2.2.1 Construction

A general half-bridge circuit with N-channel MOSFETs is shown in Figure 2-9.

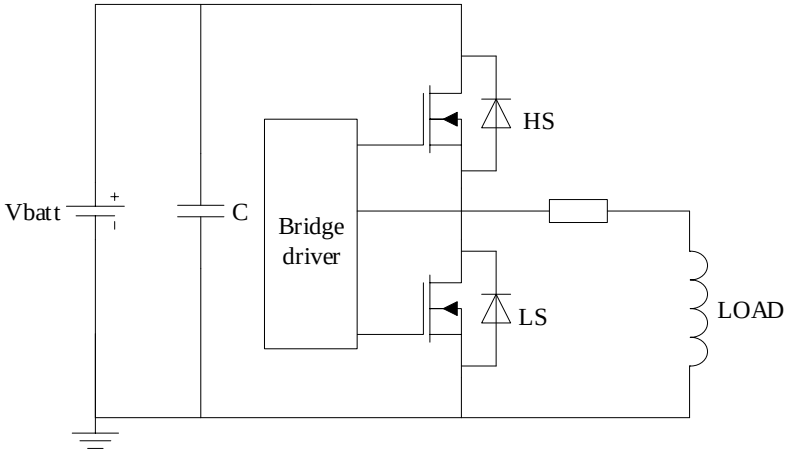


Figure 2-9: Half-bridge circuit

The half-bridge circuit can be realized for example on printed circuit board (PCB), on LTCC, on HTCC or on direct bonded copper substrate (DBC). Nowadays the latter is popular in power electronic applications due to its high thermal conductivity. In this project, I decided to use a PCB realization, because its production was faster, and this one is the lowest priced implementation.

The circuit is supplied by a DC voltage source (V_{batt}). There is a capacitor parallel with it. It stores the energy required by the switching process. It eliminates the bouncing of the battery voltage. This capacitor is usually electrolytic, because these have a large capacitance (in order of 1000 microfarads) unlike ceramic capacitors. The other reason is

that the electrolytic capacitors' resonant frequency is in order of 10-100 kHz (the impedance is the smallest here), the typical switching frequency range of driving specific bridges, and it leads to reduced dissipation.

The two MOSFETs are usually mentioned as high-side (HS) and low-side (LS). The body diode of these devices can be used for freewheeling.

In this example, the load is connected between the ground and the common point of the MOSFETs (phase output point). The load can be inductive (the inductance of it is dominant) or resistive (its resistance is dominant), but in real applications, it is always important to note both of the parameters. For example, a coil has resistance because of the resistance of the wire, and a resistance has an inductance due to the windings. When the load is inductive, it is important to note that the magnetic field needs time to build up to its final state in the coil. In this project, I used a resistive load (see in Chapter 3.4.2).

2.2.2.2 Bridge driver

The switching of the half-bridge is controlled by a driver logic. The goal is to generate high enough G-S voltage for the MOSFETs to switch on, with appropriate timing, without generating cross conducting. There are more options to realize it.

The most obvious solution is to use two independent devices (for example function generators) to generate the required signals. This solution is not practical, because the switching times have to be adjusted manually. The critical parameter is the dead time (the time between the state when one of the MOSFETs is off, and the other is not on yet), which have to be long enough to avoid shoot through. Short circuit detection have to be solved manually in this case. Additionally, the usage of two controlling devices causes the increasing of the costs.

Another option is to control the switching with software, for example by using a microcontroller. In this case, the first task is to interface the controller with the half-bridge. Error detection and handling is also programmable. Nowadays there are specific microcontrollers for this purpose, so it is a convenient solution.

There are a lot of integrated circuit solutions, too. Specific bridge driver integrated circuits are available. These usually need some additional devices (see in Chapter 3.2.2), but the operation is automatic. Error detection and handling is usually built in these devices. I use this option in this project, too (see in Chapter 3.2).

2.2.2.3 Parasitic effects in half-bridge circuits

Identification of parasitic effects is a really important topic in every electronic application. The goal of this diploma thesis is reviewing the parasitic effects related to the topology through the example of half-bridge circuits. The problem is that the conductive paths of the layouts have parasitic self-inductance, -resistance, -capacitance, mutual conductance, inductance, capacitance, coupling etc. The resistive parameters (resistance and conductance) influence mainly the power dissipation. The reactive parameters (inductance and capacitance) have effects on switching times and switching losses via generating transients even with resonance and ringing. These effects have to be considered and calculated by planning and by testing of operation, too. My goal was to create a testable construction in which I can observe and determine (or estimate) the parasitic effects and parameters.

It is important to note, that not only the layout has parasitic effects. For example in an overall planning procedure, it is necessary to analyze the capacitances of the MOSFETs, the connectors, etc. These parameters can be more significant than the layout related effects, but in this thesis, I focus only on the effects related to the topology.

3 Designed circuits

In the next chapters, I would like to summarize the design process by overviewing the circuit schematics, the layouts and finally the operation of the half-bridge circuits. I also would like to explain, how I wanted to ensure the most appropriate circumstances to focus only on the layout related parasitic effects.

3.1 Aspects of planning

Every electrical component have parasitic parameters that have to be considered. Based on general experience, manufacturing can have a more significant impact on the parasitic effects than topology. Additionally, for example, the capacitances of the MOSFETs can also be different in case of two different samples of the same devices due to the manufacturing tolerances, and this difference can be more dominant, than the layout related effects. It is especially true, when the parasitic effects are reduced intentionally (for example by minimizing the length of narrow conductive paths of the layout). Obviously, in real applications this is the goal, so in case of that, the parasitic effects related to the manufacturing are usually more significant than the layout related effects. This however does not mean that the layout related effects are negligible. To escalate it, I made intentionally ‘bad’ PCB design (for example with unnecessarily long wires), so the layout related parasitic effects became more apparent.

I designed three layouts with different topologies based on the same half-bridge circuit schematic. Each variant of the different topologies was designed so that it enhances and magnifies different parasitic effects. To minimize the differences caused by the production tolerances of semiconductors, I used the same pair of HS and LS MOSFETs in all the circuits by the measurements. To support the procedure of soldering, I designed a special footprint to the D2PAK case (Figure 3-1). I placed a relatively big plane on the bottom side of the PCBs (blue). This and the thermal vias (green) make the soldering faster, because the whole surface of the device can be heated from the bottom side of the PCB.

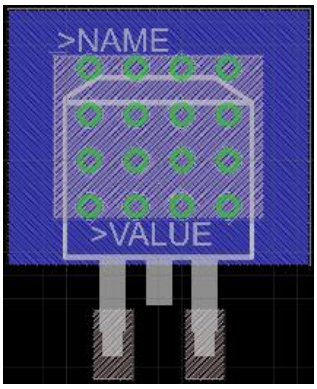


Figure 3-1: MOSFET D2PAK (TO263) footprint

The radial leaded electrolytic capacitor (hereinafter Ecap), which is populated on the half-bridge boards (see in Chapter 3.3.1), was also the same in case of every layout.

The bridge driver circuit is realized on a single board (see in Chapter 3.2). It can be connected to the half-bridge boards through pin headers. There is a pair of pin header on the driver board, and also a pair on the layout variants. With this construction, I wanted to ensure more similar testing circumstances by using the same driving logic in case of every layouts. The pin headers and the power connectors for both the power supply and the load are fix on every single half-bridge layout variants. Of course, these are not ideal components either, but these do not have considerable influence on the layout related parasitic effects, so I did not change them.

The arrangement of the components can be seen in Figure 3-2. The bridge driver board is fix, the exchangeable half-bridge components are the MOSFETs and the Ecap.

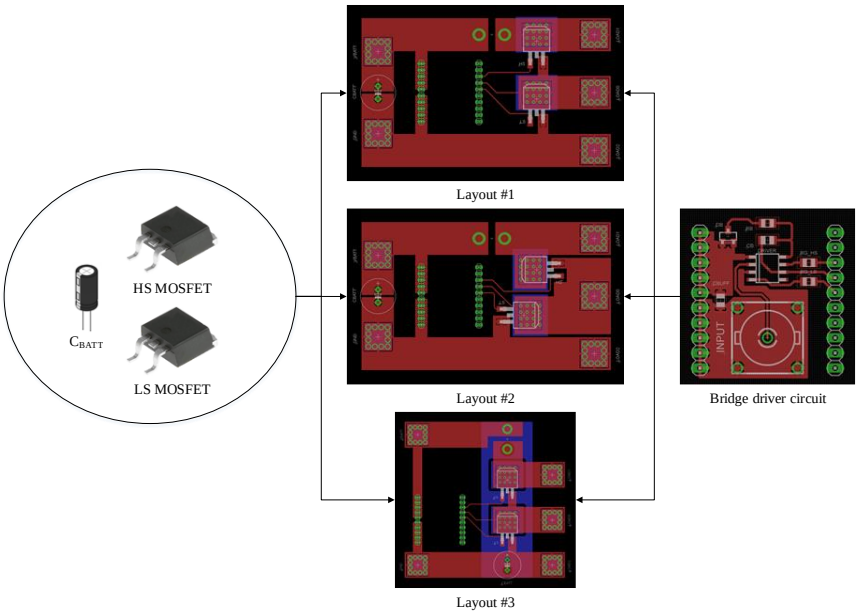


Figure 3-2: Layouts and components

With this concept, my goal was to ensure that only the layout is different between each topology variants. Every other factors are exactly or approximately (i.e. pin headers and connectors) equivalent. I made the schematic and the layouts with the designer software called Eagle 6.5.1.

3.2 Bridge driver circuit

3.2.1 Bridge driver IC

I used an integrated bridge driver circuit. The Onsemi NCP5111 is a high voltage power gate driver providing two outputs for direct drive of 2 N-channel MOSFETs arranged in a half-bridge configuration [4]. The pinout of the SOIC-8 case is shown in Figure 3-3.

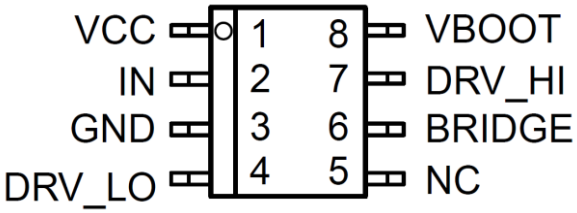


Figure 3-3: Onsemi NCP5111 pinout [4]

The device needs a supply voltage between 10 and 20 V (I used 12 V like at the half-bridge circuits), connected between VCC (1) and GND (3). The output signals are connected to the gates of the MOSFETs on DRV_HI (8) and DRV_LO (4) pins through external gate resistors. These resistors modify the switching times (see in Chapter 3.4.2.3). According to the datasheet, the DRV_HI (7) pin has to be connected to the phase output point of the half-bridge.

As an input signal, the IC receives a square wave on pin IN (2). The switching process is controlled by the parameters of this signal: frequency, amplitude, offset, phase and duty cycle. The G-S voltage of the HS power switch is in phase with the input signal, so when the input signal is high, the HS MOSFET is opened. The LS MOSFET is opened for the low level of the input signal, as it is shown in Figure 3-4.

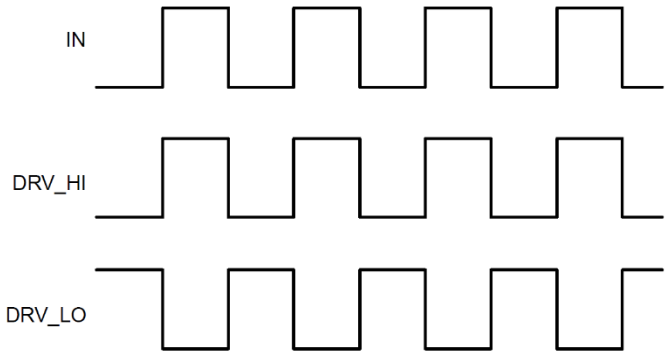


Figure 3-4: Onsemi NCP5111 signals [4]

Of course, the switching does not occur immediately, the signals have rise and fall times, and between them dead time is implemented to avoid cross conduction, as it is shown in Figure 3-5.

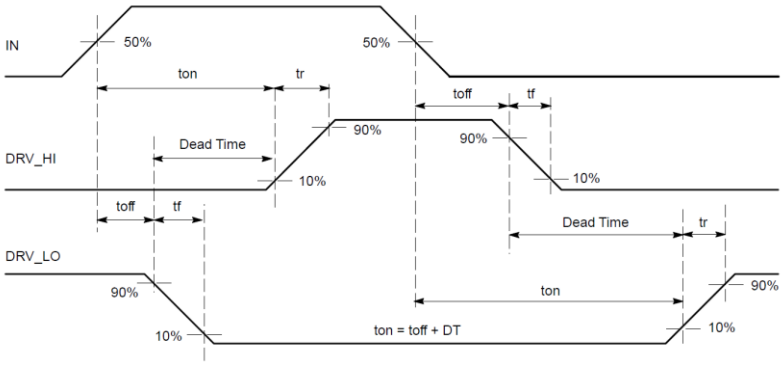


Figure 3-5: Onsemi NCP5111 timing [4]

3.2.2 Bootstrapping

Switching on the LS MOSFET is simple, because the source is connected to the ground, so the G-S voltage is the voltage between the gate and the ground. When LS is on, the potential of HS source (and so the phase output) is closely equal to ground. When the LS MOSFET turns off, the potential of HS source starts floating. HS MOSFET also needs positive GS voltage to switch on. It means, that the potential of HS gate have to be higher compared to the source potential of HS. The required charge to increase the HS gate potential is stored in the bootstrap capacitor. This capacitor gets charged to the power supply voltage through a diode and a resistor when LS is turned on (shown in Figure 3-6). Due to this capacitor, sufficient HS G-S voltage can be produced to open the HS MOSFET. This technique is called bootstrapping, and is supported by the driver IC. The bootstrap diode, resistor and capacitor are external components.

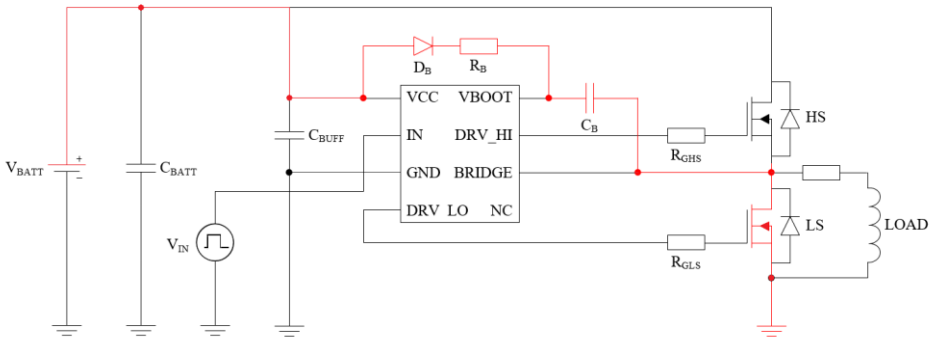


Figure 3-6: Charging of the bootstrap capacitor

3.2.3 Schematic

The schematic of the bridge driver circuit is shown in Figure 3-7.

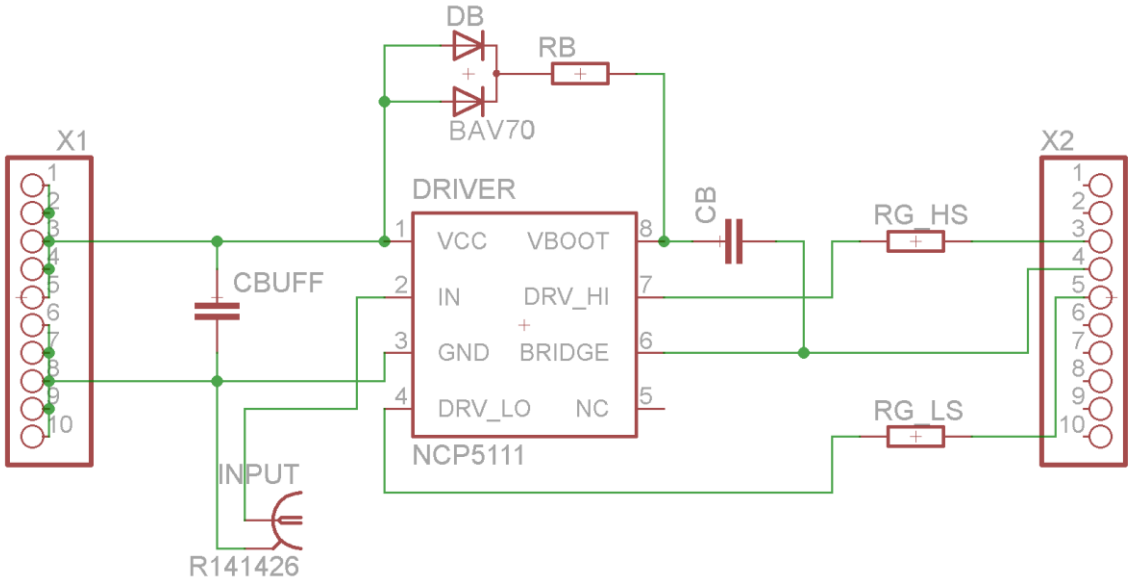


Figure 3-7: Bridge-driver circuit schematic

X1 and X2 are the 10×1 pin headers mentioned earlier. These allow connecting the bridge-driver circuit to the half-bridge PCBs with the different layouts. As I mentioned above, I built the circuit around the chosen driver IC. The DC voltage source connects to the board through X1 pin header (5 pins for the power supply, and 5 pins for the ground). It is buffered by a 1 µF ceramic capacitor.

The bootstrap diode is a Nexperia BAV70 double, common cathode diode with short recovery time to make the switching procedure faster. A 10 Ω resistance follows it in series to limit the value of the charging current. The bootstrap capacitor is connected between the bootstrap pin and the phase output. Its value is 220 nF, and it is a ceramic

capacitor. I chose the value of these components by using the recommended values of the driver IC's datasheet.

A coaxial BNC connector receives the input square wave. It seemed to be the most practical, because the function generators usually have a BNC output.

The output pins are DRV_HI and DRV_LO, these have to be connected to the gates of the MOSFETs. The gate resistors are placed on the driver board. These can also be replaced easily.

The PCB layout of the bridge-driver circuit is shown in Figure 3-8. The board's size is 3×3 cm, it is compact and easy to connect to the half-bridge circuits. Parasitic effects can certainly exist on the driver board as well, but those can be neglected as the output signals of this board are used as a reference for the measurements.

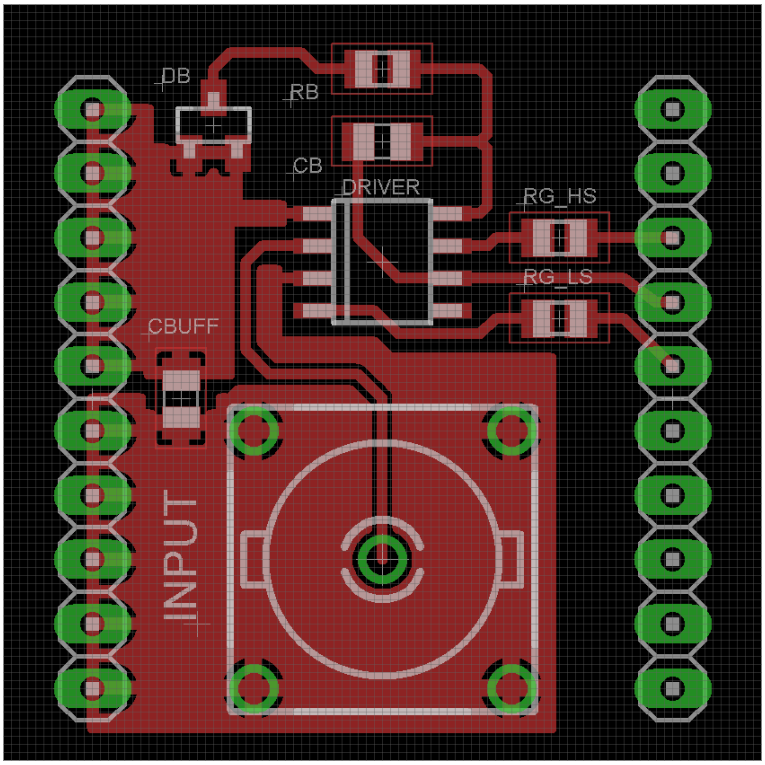


Figure 3-8: Bridge-driver circuit layout

3.3 Half-bridge circuits

3.3.1 Schematic

The schematic of the half-bridge circuits is shown in Figure 3-9. I realized three different layouts based on it.

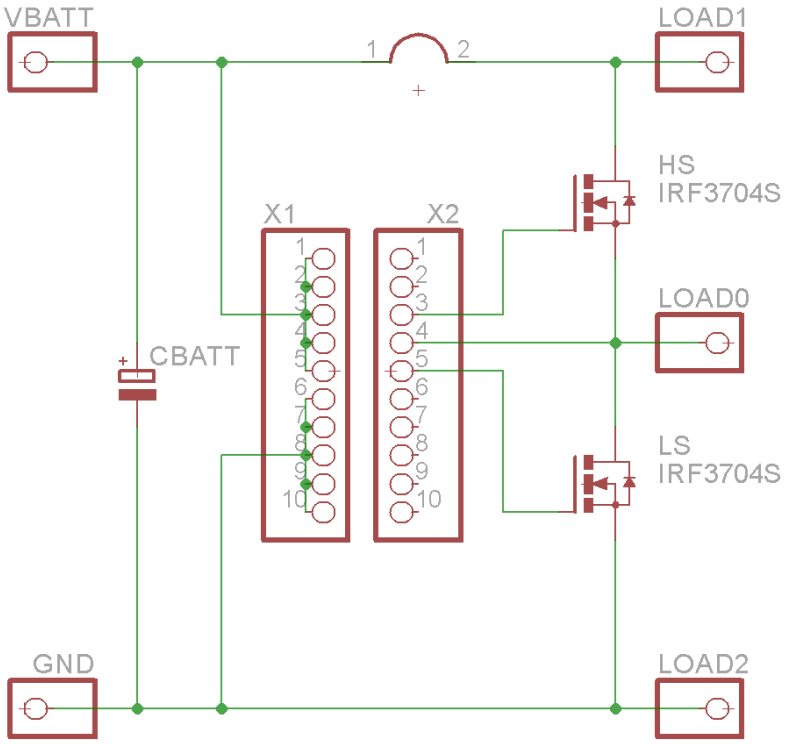


Figure 3-9: Half-bridge circuit schematic

There are five press fit bush connectors in the circuit (shown in Figure 3-10). Two for connecting the power supply (named with VBATT and GND for ground), and the other three ensure the possibility to connect the two-pole load in two different ways. Clamped cables can be connected to them with screws.

Figure 3-10: Press fit bush connector

The same electrolytic capacitor is populated on every single half-bridge board. It is an aluminum electrolytic capacitor with 1000 µF capacitance. As I mentioned earlier, it stores the energy required by the switching procedure and eliminates the bouncing of the power supply. This capacitor is also the same device in case of every layouts, like the

MOSFETs too, in order to ensure the similar circumstances. Of course, it could be placed on the driver board, too. There are more reasons that this device is on the half-bridge boards. Its size is one of the reasons: if I placed the Ecap on the driver board, it would be double sized. The most important reason is that with the position of the Ecap, the parasitic effects can be modified. The further the capacitor to the half-bridge is, the more significant the inductance of the supply wires is. That is why in real applications the Ecap is as close to the half-bridge as it can be.

The receiving 10×1 pin header pair is also placed in the circuit. These pins are connected to the appropriate points of the circuit.

I had to plan the measurements meanwhile planning the PCBs, because I had to configure the proper connecting possibilities of the devices, especially the Rogowski coil (introduced in Chapter 7). I decided to cut off the PCB's wires and place there two high diameter holes. Thus, a piece of wire can be soldered between the battery connector and the drain of the HS MOSFET in an arc of a circle, making place under it for the wire of the Rogowski coil to measure the current. This solution also ensures the possibility of modifying the parameters of this conductive path with the radius of the wire.

It can be seen, that the circuit is really simple. The most important part of the design was the configuration of the topologies.

3.3.2 Topologies

In this chapter, I would like to introduce the three different topologies based on the same circuit schematic introduced in the previous chapter. Probably, it is more effective to analyze the differences between the layouts. The layouts #1 and #2 are really similar; layout #3 is a bit different from the other ones. The size of the bridge driver circuit had to be considered during the design. I made an effort to create the layouts aesthetic and symmetric, where it was possible. The distance between the two pin headers was given, and I used this distance between other devices, too.

Layout #1 is shown in Figure 3-11. It can be seen, that the Ecap is far away from the MOSFETs, that are below each other. The power wires and lands (the polygon-shaped conductive paths) are wide, because of the high currents (the self-heating is lower due to it). The signal wires of the bridge-driver are thin, because these do not have to conduct large currents. These are not as significant parts of the parasitic analysis, as the wires and lands of the driver board.

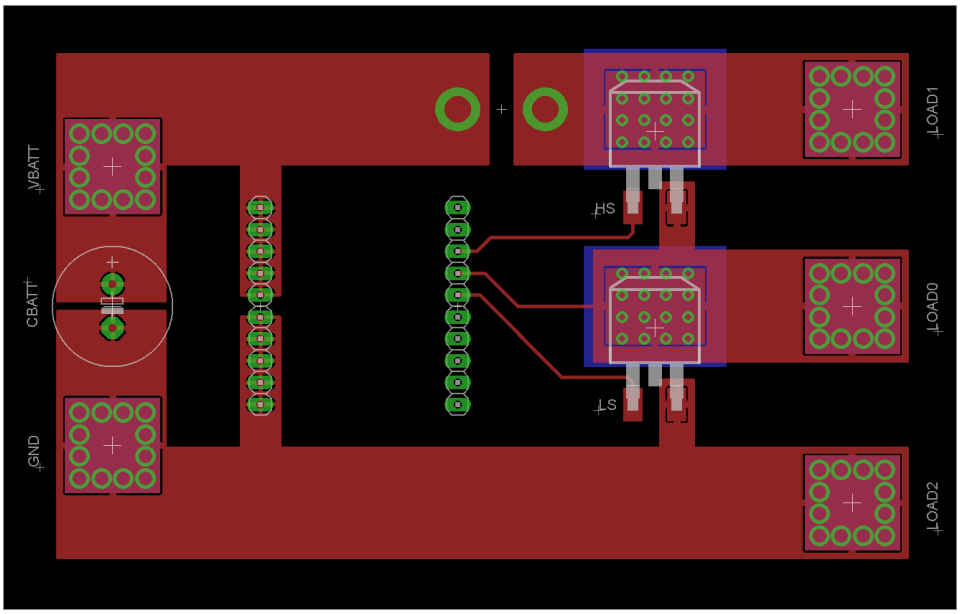


Figure 3-11: Half-bridge layout #1

Layout #2 is shown in Figure 3-12. I modified layout #1 only a bit, rotated the MOSFETs with 90 degrees. The other components' place is the same, some of the the wires and lands are modified.

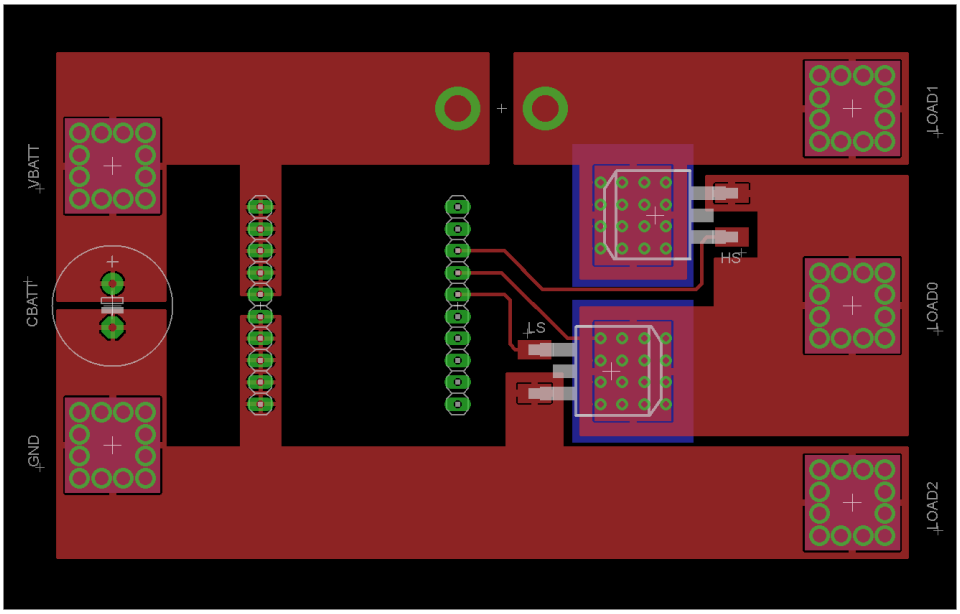


Figure 3-12: Half-bridge layout #2

Layout #3 can be seen in Figure 3-13. It was designed also with the modification of layout #1, too. The placing of the MOSFETs and connectors is almost the same. The place of the Ecap changed. It is really close to the half bridge in this layout. Besides this, I used a plane on the bottom side of the board, connecting the Ecap's positive pin to the power supply wire.

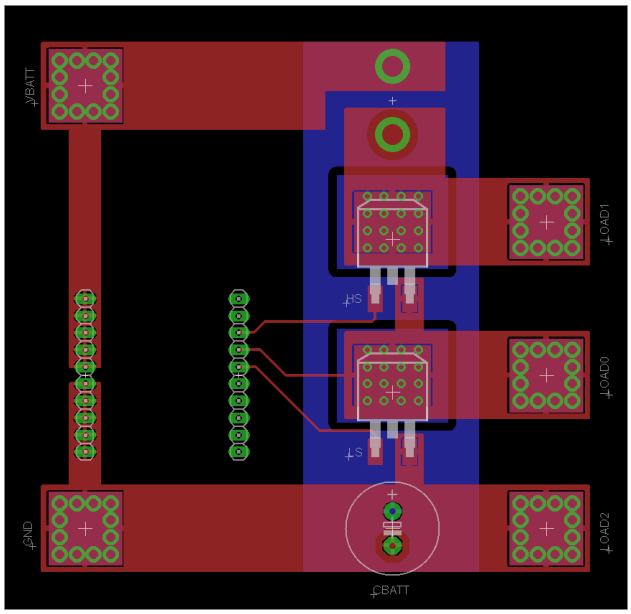


Figure 3-13: Half-bridge layout #3

I expected that the operation of this circuit is going to show different characteristics in some ways like the others. At first, the Ecap is nearer to the half-bridge means the reduction of parasitic inductance. Additionally, the 'sandwich' structure (there is a plane on the bottom side parallel with the top layers) causes a capacitance that can virtually decrease the inductance of the loop. I am going to highlight this effect in Chapter 8, when I am introducing the results.

3.4 Demonstration of ideal operation

3.4.1 Circuit schematic

In this chapter, I am demonstrating the ideal operation of the designed half-bridge circuit(s). I performed the simulations with Cadence's OrCAD PSpice. The OrCAD Capture schematic of the ideal circuit is shown in Figure 3-14. 'Ideal' means, that I ignore the layout related parasitic effects in this case. I used the model of the bridge driver IC, the diode and the MOSFETs provided by the manufacturer. The parasitic effects of these devices are implemented in the models. The proper connection of the bridge driver can be seen in the figure. In this case, I used 0 Ohm gate resistors.

The input signal is a square wave, with amplitude of 10 Volts (it is high enough to open the MOSFETs), 20 kHz switching frequency (50 µs period time) and 70% duty cycle.

I placed the series RL model of the load I used by the measurements, too, in the circuit. I wanted to have a current between 10 and 15 Amps. The RMS value of the current can be calculated by Equation 3-1, where d is the duty cycle of the input square wave, and so the current.

$$I_{RMS} \cong \sqrt{d} \cdot \frac{V_{batt}}{R_{LOAD}}$$

Equation 3-1: RMS of current

The input square wave's value can be adjusted between 10% and 90% with 10% steps by the function generator I used. Calculating with maximal (90%) duty cycle, and 15 A current, the required resistance is presented by Equation 3-2.

$$R_{LOAD} \cong \sqrt{d} \cdot \frac{V_{batt}}{I_{RMS}} = \sqrt{0{,}9} \cdot \frac{12}{15} = 0{,}76\ \Omega$$

Equation 3-2: Calculation of load resistance

I realized this resistance by connecting wire wound resistors parallel (see in Chapter 'Measurement setup' in the Appendix). I measured the parameters of its series RL model with an RLC meter. The resistance is 750 mΩ, and the inductance is 1.5 µH. It means that this is a resistive load.

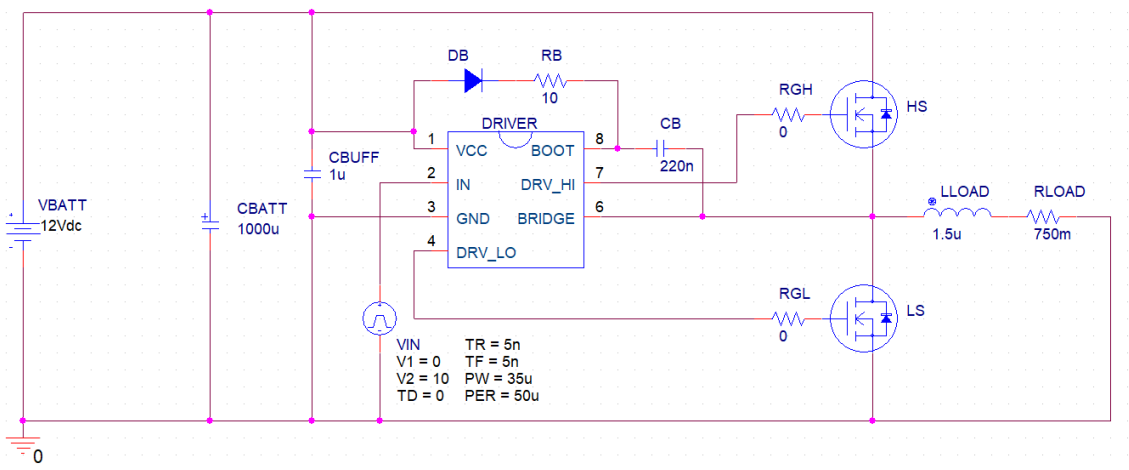


Figure 3-14: Ideal circuit schematic

3.4.2 'Ideal' characteristics

The proper operation of the bridge driver IC is shown in Figure 3-15. It can be seen, that the G-S voltage of the HS MOSFET is in phase with the input square wave. The G-S voltage of the LS MOSFET and the input signal are antiphase. The proper delay and dead times also can be seen.

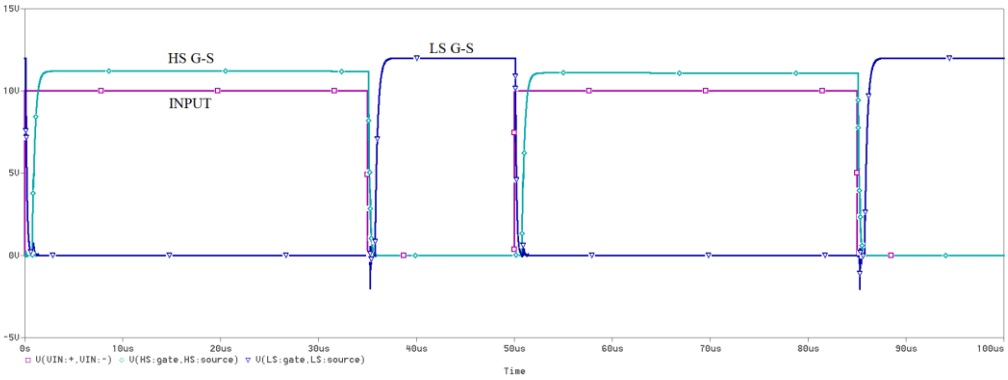


Figure 3-15: Operation of the bridge driver

The current of the load and the G-S voltages are shown in Figure 3-16. When the HS MOSFET conducts, the current flows through it and the load. The setting at rising edge is exponential, and one period is enough to achieve its maximal value due to the low inductance. When the input signal is zero (and so the LS MOSFET conducts), the active freewheeling occurs. It can be seen, that the current decreases to zero.

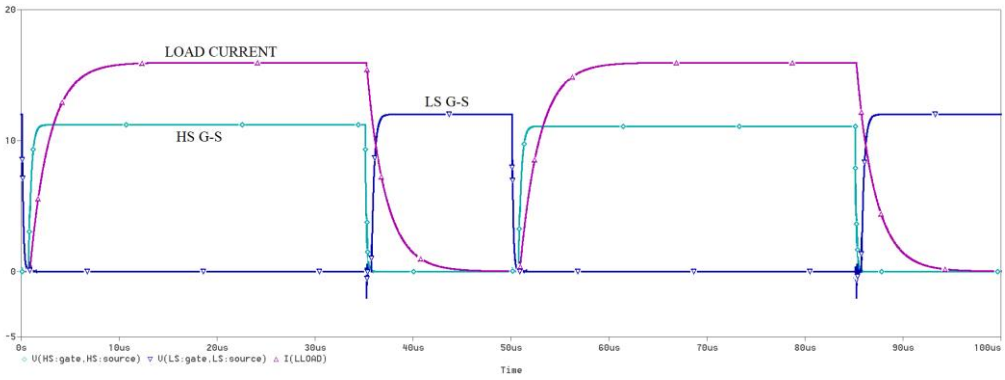


Figure 3-16: Input signal and load current

The switching transients are shown in Figure 3-18. The falling of the load current is exponential, but the current of HS drain decreases to zero after a fast and short ringing immediately. In the linear region of the falling, the inductances of the system can be estimated. I am introducing this method in Chapter 4.4.2.

The D-S voltage of the HS MOSFET can also be seen in Figure 3-18. It is important to note that the maximal value of it is a critical parameter of the device. It is temperature dependent, and is given by the datasheet (as it is shown in Figure 3-17). This is one of the main reasons that the parasitic effects have to be analyzed. The inductance of the wires can cause a high amplitude ringing in the D-S voltages. It is not significant in this case, because the inductance of the system is low, but in case of the designed boards, it is more dominant. Occasionally this voltage can be so high that the MOSFET breaks down. It causes a short circuit, and in the next switching period cross conducting

occurs, which can not be tolerated. To avoid it, it has to be ensured that the ringing amplitude of the D-S voltages do not pass the critical value. It can be ensured by decreasing the inductance of the loop.

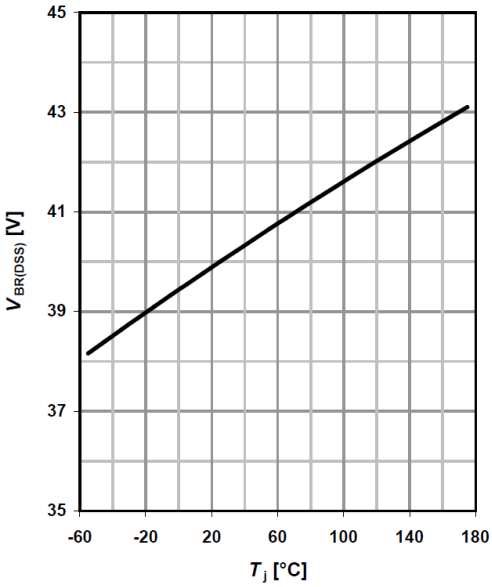


Figure 3-17: Temperature dependency of the breakdown D-S voltage [5]

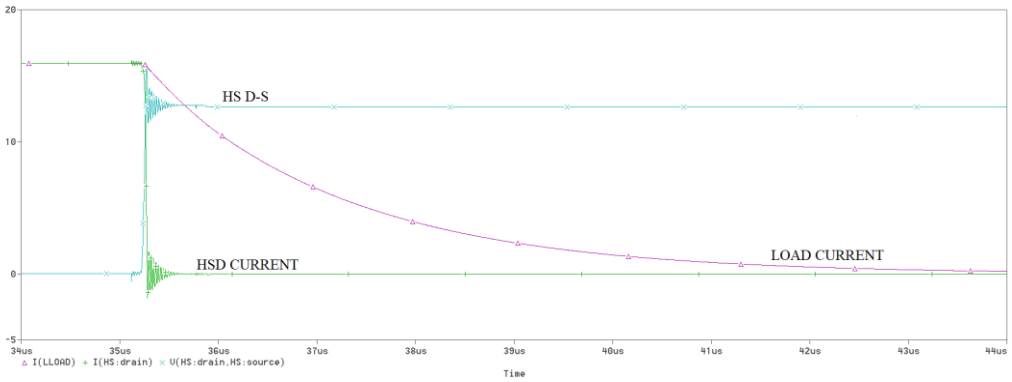


Figure 3-18: Switching transients

It is important to note that the voltage ringing can be measured not only between the MOSFETs' drain and source, but also between other points of the circuits. Of course, in this case it has no point, because the layout is considered as ideal. For example, assume that the wire between the power supply connection point to the electrolytic capacitor and the drain of the HS MOSFET is not ideal. It can be modeled with a simple series RL two-pole. In this case, induced voltage can be observed between the two mentioned points in the moment of switching. These characteristics are in the focus of the measurement and the simulations, and are compared in Chapter 8.

3.4.2.1 Bootstrapping

Let’s analyze the operation of the bootstrap circuit. The voltage of HS gate, HS source (the phase output) and the voltage between these two points are shown in Figure 3-19. It can be seen, that the source voltage is higher than zero, and due to the charges of the bootstrap capacitor, the gate voltage is higher than the power supply voltage (12 V). Thus, the voltage between gate and source is high enough to open the MOSFET. The operation is proper.

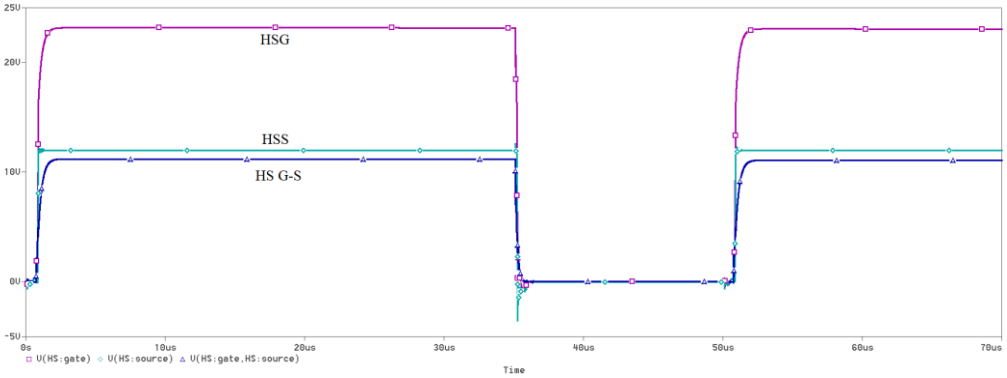


Figure 3-19: Bootstrapping

3.4.2.2 Freewheeling

To observe the difference between active and passive freewheeling, I modified the circuit by grounding the gate of the LS MOSFET. It causes that the freewheeling can only be passive, and the current can flow only through the intrinsic diode of the device in the second state.

In Figure 3-20 it can be seen that the decreasing is faster in case of passive freewheeling (with blue color), because in this case the resistance is higher (there is not a low channel resistance parallel with the diode), so the dissipation is higher also, and that is why the current decreases to zero faster. The difference is not significant in this case, due to the low inductance of the load.

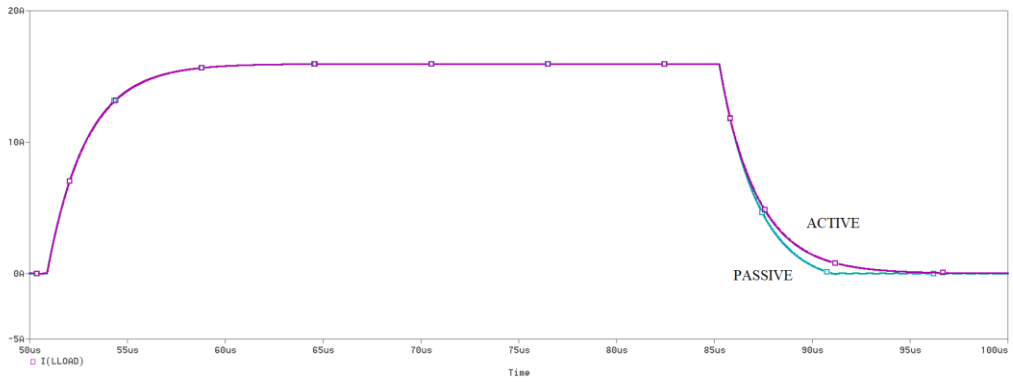


Figure 3-20: Active and passive freewheeling

3.4.2.3 Effect of the gate resistors

I used 0 Ohm gate resistors in the above-mentioned example. In this case, I modified the value of R_{GH} to 60 Ω and R_{GL} to 100 Ω. I note that the maximum values are 60 Ω and 20 Ω according to the datasheet. I wanted to see, what happens, if I set higher values. The difference between the switching processes compared to the former ones can be seen in Figure 3-21. The new curves have a point of intersection at approximately 3.8 Volts. The possibility of cross conducting is grown. That is why the resistance of the external gate resistors is limited. These limits have to be considered, because in the opposite case, the avoiding of cross conduction is not warranted.

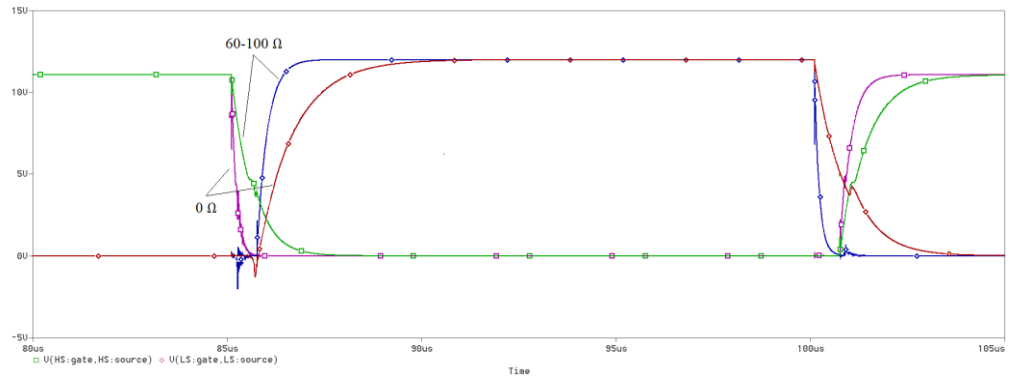


Figure 3-21: Effects of the gate resistors

3.4.2.4 Load connected between power supply and phase output

In the examples until now, the load was connected between the phase output and the ground. The input signal and the current of the load in case that the load is connected parallel with the HS MOSFET is shown in Figure 3-23. The circuit schematic can be seen in Figure 3-22. The operation is opposite to the previous: high current flows through the load (with opposite direction of flow), when the LS MOSFET is opened, and freewheeling occurs in the other state.

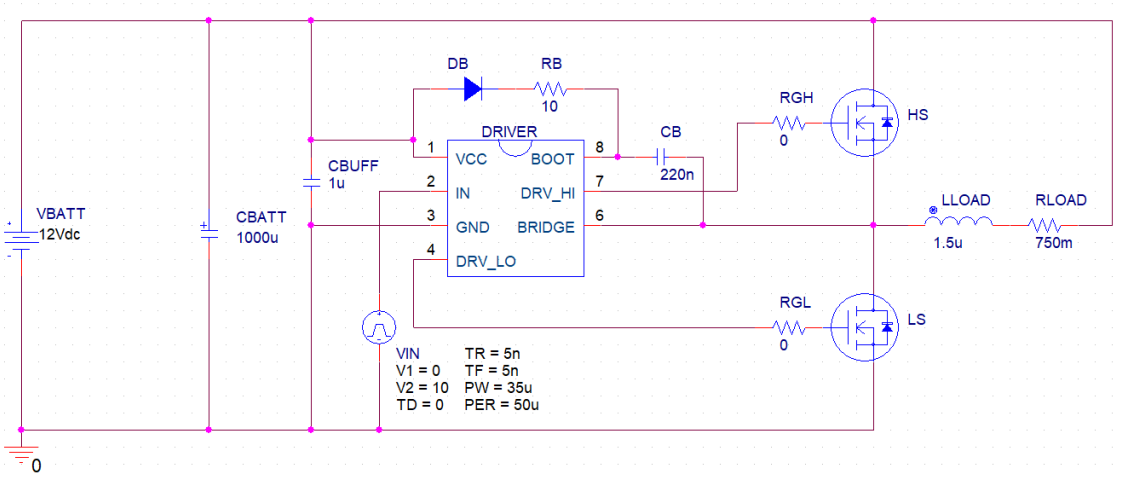


Figure 3-22: Ideal circuit schematic, load between power supply and phase output

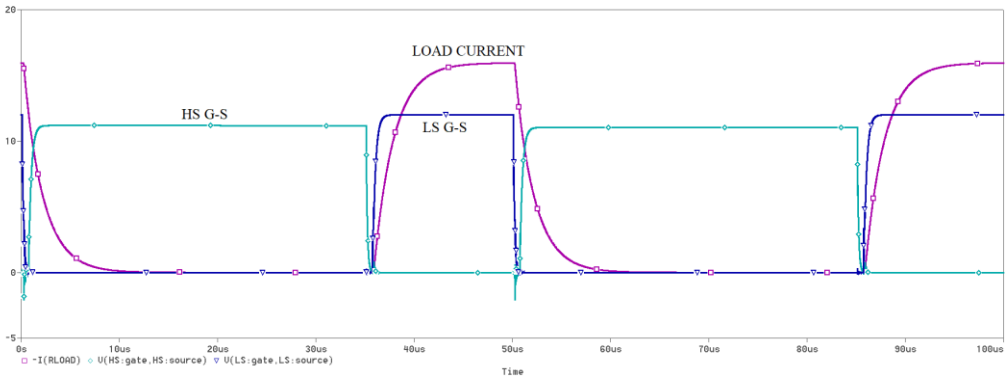


Figure 3-23: Load connected to HS

In the previous chapters, I summarized the characteristics of the ideal operation. In the later chapters, this model is going to be complemented with incorporation of the parasitic effects.

4 Parasitic analysis in power electronics

4.1 Basics of parasitic analysis

The classic example to introduce the significance of parasitic analysis is that the simplest discrete electrical components, like resistors, inductors and capacitors are not ideal. These components have parasitic parameters that have to be considered while using these devices. For example, a winded resistor has inductance and capacitance, a coil's winding has resistance and capacitance, a capacitor has series and parallel resistance, inductance, and so on. These effects are usually implemented in lumped element models, which means that the models of the devices consist of simple R, L, C components.

The propagation velocity of electric signals is in order of the velocity of light, which is $3 \cdot 10^8 \frac{m}{s}$ in vacuum. Additionally, in power electronics the operating frequencies are usually in order of 10-100 kHz. The highest considered overtones are usually in order of 10-100 MHz. It means, that the minimal wavelength (λ) is on order of meters, which is usually larger at least one order of magnitude, than the characteristic length (L), which is the largest linear dimension of the parts of the electrical circuits (components, conductive paths, etc.). According to it, the propagation can be considered as instantaneous. That is why the systems can be modeled with circuits containing lumped element multi-poles. Equation 4-1 presents the mathematic expression of this rule of thumb.

$$L \leq 0{,}1 \cdot \lambda$$

Equation 4-1: Rule of thumb for umped element models

Systems operating at high frequencies (for example radio frequency applications, like antennas) and containing large-dimensional elements (for example power transmission and power distribution network), can only be modeled with distributed parameter models, because the wavelength can be commensurable with the linear extensions of the elements.

Every elements of an electrical circuit has parasitic parameters. The goal of this thesis is to review the possibilities of identification and modelling of layout related parasitic effects in power electronics, and choose the one(s) that converge(s) to measurement results mostly. I am introducing the analyzed methods in the next chapters.

4.2 Estimations, analytical approximations

According to the above-mentioned considerations, I use simple lumped element two-poles to model the parasitic effects of the conductive paths of the PCBs. Explicit analytical formulas can be figured out for resistance, inductance and capacitance by using the theory of electromagnetic fields. These formulas are derived by using approximations and neglecting some non-ideal effects. Geometry limits also have to be considered. In this project, I assume that the materials of the mediums mentioned are homogenous, isotropic and linear (ρ, σ, μ and ε are constants).

4.2.1 Resistance

4.2.1.1 DC resistance

The resistance of a conductor depends primarily on two factors: its material, and geometry. The material has a specific conductance (σ). Its unit is Siemens/m (S/m). Its reciprocal, the specific resistance (ρ) is also often used. Its unit is Ωm. These parameters can depend on temperature, frequency, etc., but in this project, as I mentioned above, I assume, that these are constants.

Assume that direct current flows through the conductor. In this case, the current density is homogenous through the whole volume of it. The resistance is proportional to the length of the conductor (l), and inversely proportional to the cross-section area (A). The DC resistance of a conductor with constant cross-section through the length of it can be derived from Equation 4-2.

$$R = \rho \cdot \frac{l}{A} = \frac{1}{\sigma} \cdot \frac{l}{A}$$

Equation 4-2: DC resistance

The DC resistance of a rectangular cross-sectioned conductor with length l, width w and thickness t, is presented by Equation 4-3.

$$R = \rho \cdot \frac{l}{w \cdot t} = \frac{1}{\sigma} \cdot \frac{l}{w \cdot t}$$

Equation 4-3: DC resistance of a conductor with rectangular cross-section

The DC resistance of a conductor with circular cross-section is presented by Equation 4-4. Its radius is marked as r in the formula.

$$R = \frac{1}{\sigma} \cdot \frac{l}{r^2 \pi}$$

Equation 4-4: DC resistance of a conductor with circular cross-section

These are simple formulas to derive the resistance. Homogenous current density and homogenous medium are assumed. These are valid in case of direct current, and are approximately valid at low frequencies.

4.2.1.2 AC resistance

In case of high frequency, the proximity effect and the skin effect have to be considered, while deriving the resistance of a conductor. Proximity effect appears, when alternating currents are flowing through more conductors that are nearby each other. In this case, the current distribution inside the conductors is influenced by the others' currents. It means, that the homogeneity of current density can not be assumed anymore, and so Equation 4-2 is not valid in this case.

The other significant effect in case of alternating currents is the skin effect. I do not prove this effect in this thesis, but it could be proven by using the theory of electromagnetic waves, applying the quasi-static approximation (the conducted current is higher in orders of magnitude than the displacement current) [16]. It can be observed, that at high frequencies, the current density is high near the surface of the conductor, and it decreases exponentially from the surface towards the inside. Its mathematical description is presented by Equation 4-5.

$$|J(z)| = J_0 \cdot e^{-\frac{z}{\delta}}$$

Equation 4-5: Current density considering the skin effect

J_0 is the current density near the surface of the conductor, z is the distance between the surface and the observed inside point of it. The quantity marked as δ is the skin depth. It is defined as the depth below the surface of the conductor at which the current density at the surface (J_0) has fallen to its $1/e$. The skin depth can be calculated with Equation 4-6, which is also derived by using the quasi-static approximation [16]. It depends on the frequency, and on the material parameters of the conductor. The higher the frequency is, the smaller the skin depth is.

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}} = \sqrt{\frac{2}{2\pi f \mu \sigma}} = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

Equation 4-6: Derivation of the skin depth

The skin depth is often used to approximate the skin effect in calculations. As I mentioned above, the decreasing of the current density from the surface towards the inside of the conductor is exponential (curve #1 in Figure 4-1). It is often assumed, that the current density between the surface and the depth of skin depth is constant, and is zero farther inside the material (curve #2 in Figure 4-1). The areas under the curves are equal (proven by Equation 4-7), so if we do not want to know the current density in discrete points, only the total value of it is used, this assumption is proper.

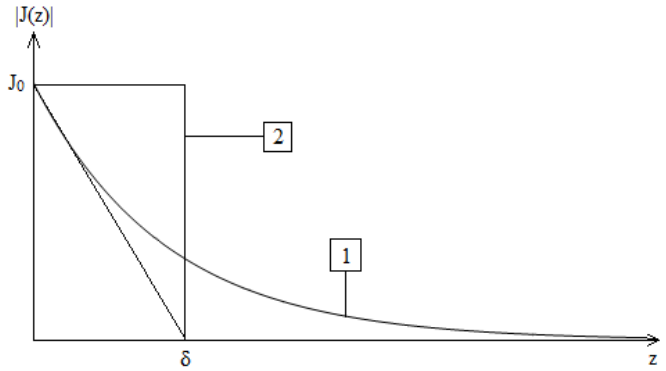


Figure 4-1: Skin depth

$$\int |J_1(z)|\,dz = \int_0^{\infty} J_0 \cdot e^{-\frac{z}{\delta}}\,dz = J_0 \cdot \int_0^{\infty} e^{-\frac{z}{\delta}}\,dz = J_0 \cdot (-\delta) \cdot \left[e^{-\frac{z}{\delta}}\right]_0^{\infty} =$$

$$= -J_0 \cdot \delta \cdot \left(\lim_{z\to\infty} e^{-\frac{z}{\delta}} - 1\right) = J_0 \cdot \delta \equiv \int |J_2(z)|\,dz$$

Equation 4-7: Approximation with homogenous current density

Of course, the skin effect, and so the frequency influences the resistance of conductors, because resistance depends on the cross-section area that the current flows through. Three different cases can be distinguished. Let's see a conductor with cylindrical cross-section. If the (in this case, theoretical) value of the skin depth is larger than the radius of the conductor, the above-mentioned DC resistance can be used, because the current flows through the whole of the cross-section. It is true in case of DC and low frequencies. If the skin depth is much smaller than the radius of the conductor, the AC resistance have to be used (see below). In the third case, when the skin depth and the radius are commensurable, analytical or numerical methods have to be used (for example Bessel's curves to estimation, or finite element simulation for more accurate results). I do not deal with this case in this thesis, because it is not common in power electronics.

The AC resistance can be derived for conductors with any shape by using the electromagnetic field's vectors (electric field, magnetic field and the Poynting-vector).

The AC resistance of a conductor with circular cross-section is presented by Equation 4-8.

$$R = \frac{1}{\sigma} \cdot \frac{l}{2r\pi \cdot \delta}$$

Equation 4-8: AC resistance of cylindrical wire [16]

Let's compare Equation 4-8 to Equation 4-2. It can be appreciated, that the cross-section area, the current flows in – according to the assumption – is $2r\pi \cdot \delta$, which is the area of a rectangle with edges length of δ (the skin depth), and of $2r\pi$ (circumference of the circle). The curvature of the surface is locally neglected, according to $\delta \ll r$.

For conductors with cylindrical cross-section, the formula is simple. For conductors with other shape of cross section, the derivation methods and the formulas are more complicated. In these cases, the finite element method provides the best solutions.

4.2.2 Inductance

4.2.2.1 External and internal inductance

Current flowing in a conductor generates magnetic field. The magnetic field has a magnetic flux. As Equation 4-9 presents, inductance (L) is defined, as the ratio of the magnetic flux (ϕ) and the current (I). Its unit is $\frac{Vs}{A} \equiv H$ (henry).

$$L = \frac{\phi}{I}$$

Equation 4-9: Definition of inductance

If the magnetic flux surrounding the conductor is generated by another conductor's current, mutual inductance can be defined between the conductors. If the magnetic flux is generated by the current of the conductor that it is surrounding, the inductance is self-inductance. Hereinafter, the word 'inductance' means the self-inductance.

Assume that the current I flows through a conductor with finite cross-section area. The magnetic flux is the flux surrounding the conductor, created by the current flowing in it. External inductance can be defined as the ratio of this magnetic flux and the current flowing in the conductor, that generates it.

$$L_{ext} = \frac{\phi_{ext}}{I}$$

Equation 4-10: Definition of external inductance

External inductance is a constant value in case of a specific conductor. DC current generates constant magnetic flux, and the ratio of two constants is also constant. In case of AC the magnetic flux is frequency dependent, but the frequency dependence is eliminated by the division in the formula.

Perfect conductors have infinite specific conductance ($\sigma \to \infty$). In these materials, the electric and magnetic field are zero: $\vec{E} = \vec{0}$ and $\vec{H} = \vec{0}$, and so the energy inside is also zero. Real conductors' specific conductance is high, but finite. It means that in these materials the electric and magnetic field are not zero. Equation 4-11 presents the magnetic energy density.

$$w_M = \frac{1}{2} \cdot \mu \cdot \left|\vec{H}\right|^2 = \frac{1}{2} \cdot \frac{\left|\vec{B}\right|^2}{\mu}$$

Equation 4-11: Magnetic energy density

The magnetic energy stored in the volume of the conductor (V) can be derived from Equation 4-12.

$$W = \int_V w_M \, dV = \int_V \frac{1}{2} \cdot \frac{B^2}{\mu} dV$$

Equation 4-12: Magnetic energy stored in volume V

The energy of the magnetic field can also be defined with the inductance and the current, as it is presented in Equation 4-13. This formula is known from network theory.

$$W = \frac{1}{2} \cdot L \cdot I^2$$

Equation 4-13: Megnetic energy expressed with inductance and current

Of course, Equation 4-12 and Equation 4-13 are equal, because both of them present the energy stored in the magnetic field. According to it, internal inductance can be defined from the energy of the magnetic field. Equation 4-14 presents the formula.

$$\int_V \frac{1}{2} \cdot \frac{B^2}{\mu} dV = \frac{1}{2} \cdot L_{int} \cdot I^2$$

Equation 4-14: Implicit definition of internal inductance

A specific conductor's internal inductance is constant in case of DC. If the frequency $f \to \infty$, the skin depth $\delta \to 0$, no internal current is linked by the magnetic field, so the internal inductance is zero. It means, that the internal inductance decreases

with frequency. Equation 4-15 presents the total inductance. It is the sum of the external and the internal inductance.

$$L = L_{ext} + L_{int}$$

Equation 4-15: Total inductance

Let's see an example to observe the frequency dependence of inductance. In this example, I used the finite element method (introduced in Chapter 4.3). I determined the inductance of a cylindrical wire with the length of 250 mm and the radius of 2.5 mm with simulation. It can be seen in Figure 4-2, that the inductance decreases with the frequency due to the skin effect's influence on the internal inductance. The final value is the external inductance, which is constant.

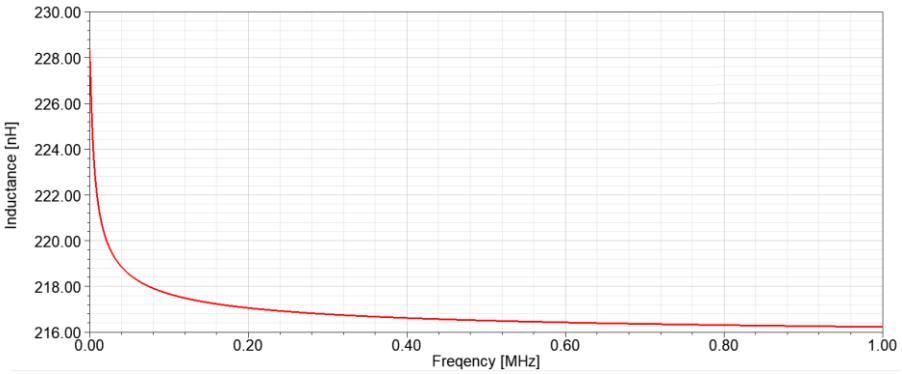


Figure 4-2: Frequency dependence of inductance

It also can be seen in Figure 4-2, that the value of the internal inductance (the difference between the start value and the finite value, approximately 10 nH) is lower by one order of magnitude than the external inductance. This is the reason, why the internal inductance is often neglected. External inductance is usually a proper approximation of total inductance.

4.2.2.2 Formula for cylindrical wire's inductance

Inductance of conductors with symmetric geometry can be derived analytically. The simplest example is the finite length cylindrical wire. It would seem that the circuit is open, so no current can flow in it. Of course, it is assumed that the other parts of the circuit are magnetically shielded, thus their inductance is zero, but the circuit is closed.

It is assumed, that the density of the DC current flowing through the wire is homogenous. The main problem is that the magnetic field is inhomogeneous at the endpoints of the wire. This is similar to the problem of parallel plate capacitors, where the electric field is inhomogeneous at the edges of the plates. The latter effect is usually

neglected. The inhomogeneity of the magnetic field is more significant, that is why it can not be neglected. The derivation method can be seen in Chapter 'Inductance of a finite length cylindrical wire' of the Appendix.

Equation 4-16 presents the inductance of a finite length cylindrical wire. It can be seen, that the formula is nonlinear. Both the length and the ratio of the length and the radius take place in the formula. Superposition is not valid in case of nonlinearity.

$$L \cong \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln \frac{2l}{r} - 0{,}75 \right), if\ l \gg r$$

Equation 4-16: Inductance of a finite length cylindrical wire

I demonstrate the nonlinearity through a simple example. Let's see a cylindrical copper wire with the length of 100 mm, and with the radius of 1 mm. Its inductance from Equation 4-16 is 63 nH. After cutting the wire at its middle point, the inductance of both half-wires is 25 nH. If superposition would be valid, the double of it would have to be equal with the inductance of the original wire. It does not obtain in this case, due to the nonlinearity.

The other problem with this formula is that it is derived by approximations. It is valid only if $l \gg r$. This is a strict condition for the geometry. Additionally, DC with homogenous density is assumed. Frequency dependence is neglected, so it is only valid in case of DC and low frequencies.

This simple example demonstrates that the using of analytically derived formulas have strict limits. Additionally, the derivation method is already complicated in case of this simple geometry, too. Equation 4-16 can be used for example to estimate the inductance of THT components' leads.

4.2.2.3 Formulas for inductance of wires with rectangular cross-section

The PCBs' conductive paths are mostly rectangular cross-sectioned conductors, as it is shown in Figure 4-3.

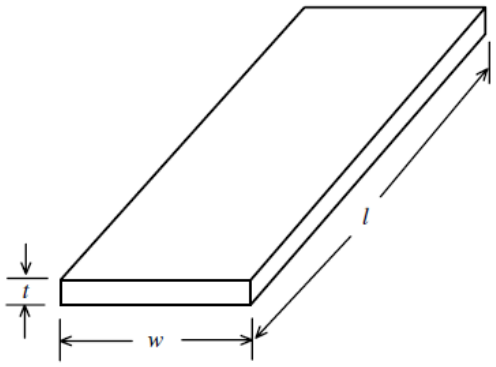


Figure 4-3: PCB land [7]

Formulas for inductance can be derived with a similar method, than in case of a cylindrical wire. If the length of the wire is much larger than its width ($l \gg w$), the inductance can be calculated by Equation 4-17.

$$L \cong \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln \frac{2l}{w} + 0{,}5 + \frac{w}{3l} \right)$$

Equation 4-17: Inductance of rectangular wire, $l \gg w$ [7]

In case of the width is larger than the length ($w \geq l$), Equation 4-18 have to be used.

$$L \cong \frac{\mu_0}{2\pi} \cdot l \cdot \frac{l}{w} \cdot \left(\ln \frac{2w}{l} + 0{,}5 + \frac{l}{3w} \right)$$

Equation 4-18: Inductance of rectangular wire, $l \leq w$ [7]

These formulas are also nonlinear, and also have strict geometry limits. Frequency dependence can also not be considered. Equation 4-17 can be used to estimate the inductance of signal wires of PCBs, but not in power electronics, where the wires are wide due to the high currents, so the $l \gg w$ geometry condition is usually not true.

4.2.2.4 Rule of thumb: '1 $mm = 1\ nH$'

The rule of thumb mentioned in the title is an often-used estimation of inductance. I note that without properly determined conditions this is not valid. Equation 4-19 formulates the rule of thumb mathematically. Let's analyze Equation 4-16 from this point of view.

$$\frac{L_{nH}}{l_{mm}} = 1$$

Equation 4-19: Rule of thumb: '1 mm = 1 nH'

$$L \cong \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln\frac{2l}{r} - 0{,}75\right) \rightarrow \frac{L_{nH}}{l_{mm}} = \frac{\mu_0}{2\pi} \cdot 10^{-3} \cdot \left(\ln\frac{2l_{mm}}{r_{mm}} - 0{,}75\right) \cdot 10^9$$

The equation is true, if:

$$\frac{\mu_0}{2\pi} \cdot 10^{-3} \cdot \left(\ln\frac{2l_{mm}}{r_{mm}} - 0{,}75\right) \cdot 10^9 = 0{,}2 \cdot \left(\ln\frac{2l_{mm}}{r_{mm}} - 0{,}75\right) = 1$$

It is exactly true, if:

$$\frac{l}{r} = 157.1$$

As it can be seen in Figure 4-4, the rule of thumb is valid only in a narrow range. The inductance per mm increases with the ratio of the length and the radius of the wire. The percent error is in a range of 10% if the ratio is between 100 and 260.

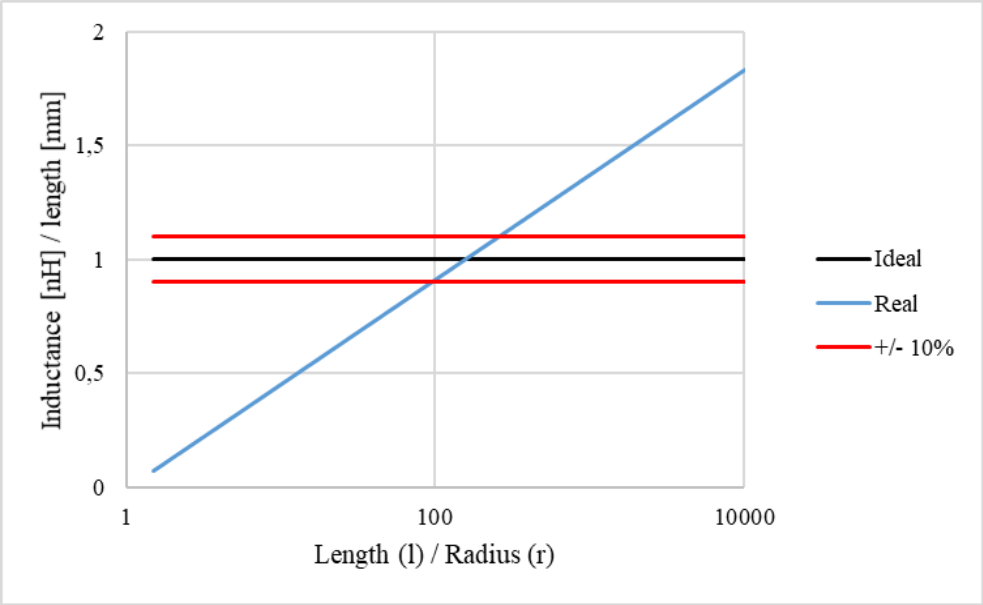


Figure 4-4: Rule of thumb in case of cylindrical wires

The case of rectangular cross-sectioned wire can be analyzed similarly. In this case, the rule of thumb is exactly true, if:

$$\frac{l}{w} = 45$$

The graph shown in Figure 4-5 is similar to the one above. The percent error is lower than 10%, if the ratio is between 25 and 75.

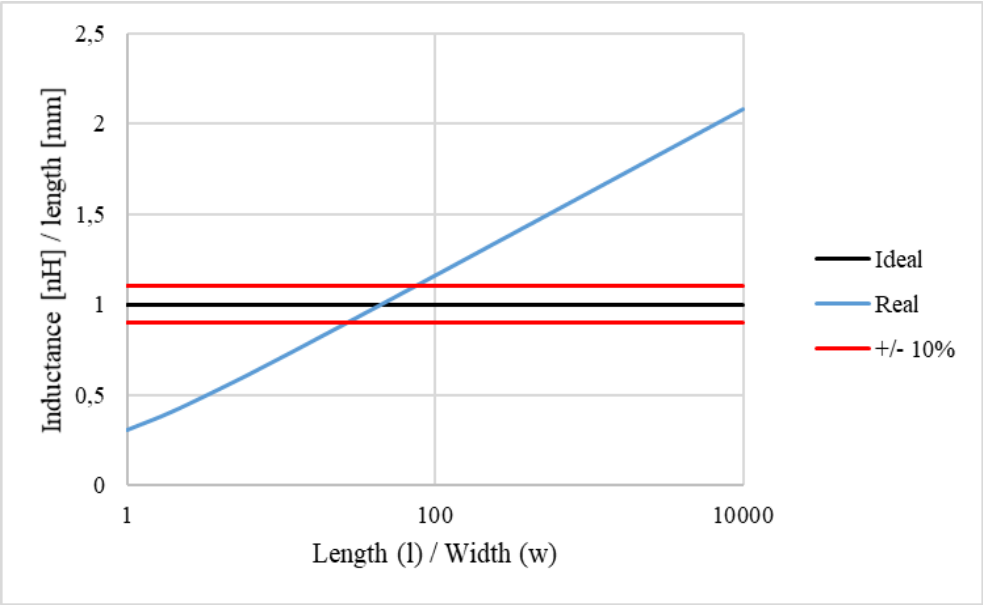


Figure 4-5: Rule of thumb in case of rectangular cross-sectioned conductor

This analysis helped me to show that the '$1\ mm\ =\ 1\ nH$' rule of thumb is valid only if the specified conditions are considered. In Chapter 5, I am introducing the parasitic analysis of the designed circuits. I derived the parameters of the models with this method, too, to demonstrate the differences between the other methods.

4.2.3 Capacitance

Besides parasitic resistance and inductance, parasitic capacitance can also appear in electrical circuits. The substrate, which separates the conductors, is an insulator with specific relative permittivity (ε_r). It can be considered as the dielectric of parasitic capacitors. The electrodes can be the conductive paths of the PCB, the leads of the components, etc.

Equation 4-20 presents the capacitance of a plate capacitor. The cross-section area of the plates is marked with A, their distance is marked as d. The formula can be used to estimate the capacitance between parallel conductor planes with the same cross-section area. The inhomogeneity of the electric field at the edges of the plates is neglected.

$$C = \varepsilon \cdot \frac{A}{d}$$

Equation 4-20: Plate capacitor's capacitance

The parasitic capacitance usually appears between relatively large expanded parts of the circuits. This is the reason why it can be more proper to use distributed parameter model instead of lumped elements. Of course, this can result more complicated models that are difficult to determine analytically. The best method to implement the parasitic

capacitance to a model is the finite element method. I am going to refer to this topic while introducing the measurement results of layout #3.

4.3 Finite element method (FEM) [3]

4.3.1 Introduction

The finite element method (FEM), or also commonly mentioned as finite element analysis (FEA), is a numerical method for solving problems linked with physical phenomenon. It is used in more fields of physics, for example in fluid flow problems, heat transfer analysis, and of course, electromagnetic problems, too. In this thesis, I focus on the latter. FEM is used in cases, in which the analytical solution of the equations derived is complicated or impossible. For example, in electromagnetics, the equations of the field are usually partial differential equations (PDEs). These are difficult to solve analytically, due to the not definitely symmetric geometry, the different aspects of excitations (the sources of the field), the inhomogeneity of the mediums, the frequency dependence, etc. The finite element method approximates the continuous functions of the field with discrete functions, based on a finite number of values.

Nowadays, the computers are indispensable part of finite element analysis. The size of the databases can not be handled manually. The development of informatics allows the development of even more effective software for finite element simulations. In this project, I used the Q3D Parasitic Extractor module of ANSYS Electromagnetics to identify the parasitic effects turning out due to the layout in half-bridge circuits. In the next chapters, I am introducing the main functions of this software module.

I note that proving the correctness of the FEM's theory is not my goal; I only use it to support my work. I only mention the properties of it that are relevant in aspect of the project. I assume a basic knowledge in theory of it.

4.3.2 Geometric models

The zeroth step of solving physical problems with finite element method is always the implementation of the device, construction, medium, etc. to a geometric model. The number of dimensions of the model depends on the complexity of the problem. Derivation of parameters per unit (for example resistance, inductance, capacitance and conductance per unit of a coaxial cable) usually requires only a two-dimensional model. Some of the

FEM software has a 2D solver specifically for these problems. General problems are usually based on three-dimensional models.

There are several possibilities to provide the geometric models. Computer-aided design (CAD) software packages with different complexity can be used to this. The geometric models are not only used as input of finite element simulations, but also are the base of manufacturing and realization. There are courses to study the theory of CAD modelling, and there are several software specific courses, too. Generally it can be declared, that the application of them requires experience. The disadvantage of them in point of electrical engineers' view is that the education of CAD modelling is not definitely part of the electrical engineering courses. This is the reason, why the workflow is often separated. The geometric modelling part of it is often executed by educated constructors or mechanical engineers.

Several of the FEM software packages has own, integrated geometric model creator and editor. These are usually simpler to use than the CAD modelers, and due to it these are not so versatile. The advantage of them is that these are parts of the software packages. It usually eliminates the file compatibility problems. The interface of the simulation and modeler modules are usually similar. It also makes the work smoother.

Space Claim is the integrated geometric model editor of ANSYS. It can be used to create 2D or 3D geometric models from the beginning, or to modify existing models. Geometry models created by external CAD software can also be modified with Space Claim. The latter is really useful, because if the models are created not by the person, who executes the FEM simulations, but an external one, the models almost always have to be modified. Its reason is that the Electromagnetics module of ANSYS is sensitive in case of touching surfaces, intersecting bodies etc. The critical situations can be handled properly, if the geometry model is created with Space Claim, but if it was created with an external software, the conversion is not always smooth. In these cases, the correction can be performed by Space Claim, too. I note that the Electromagnetics module also provides the possibility of creating geometry models, but this editor is more primitive than Space Claim.

I used Space Claim to create the models of the layouts I designed and introduced in Chapter 3.3.2. 3D geometry model of layout #1 is shown in Figure 4-6. The components (MOSFETs, electrolytic capacitor, connectors and the bridge driver board) are not parts of the model. Its reason is that I focus only on the layout.

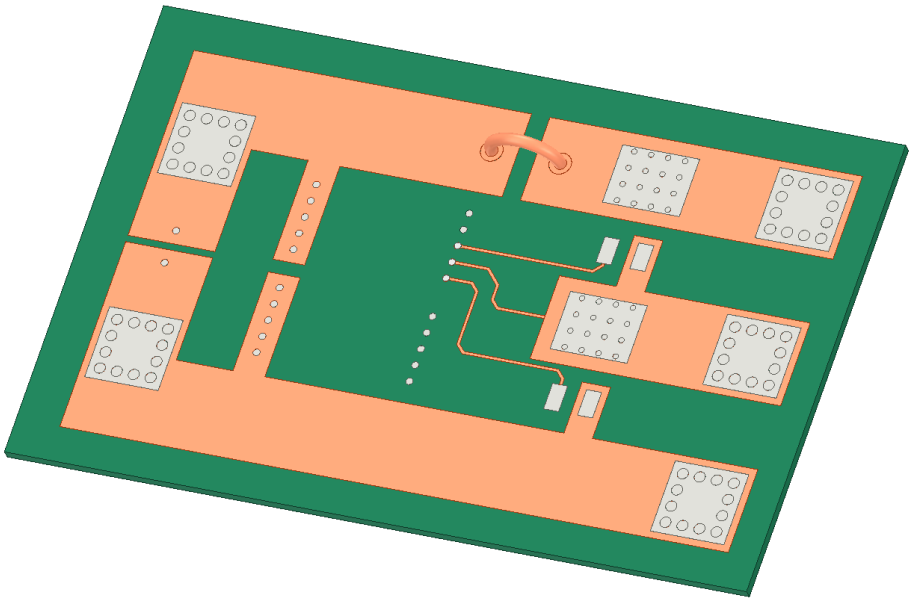


Figure 4-6: 3D geometry model of layout #1

The colors of the model can be set automatically with the option 'Material appearance'. This option is really useful in case of models with several elements, because it makes easier to check if every elements' material is set properly. I used the default, constant material parameters of ANSYS. The specific conductance of copper is $58\ MS/m$, this is the material of the conducting paths. Their thickness is 18 μm (it is specified by the manufacturer of the PCBs). The pads' material is solder, and the substrate is FR4 epoxy with the relative permittivity of 4.4.

The bottom side of layout #1 is shown in Figure 4-7. The planes and the vias that support the soldering of the MOSFETs (mentioned in 3.1) can be seen in the figure. I filled the holes with cylinders made of solder to model the soldering.

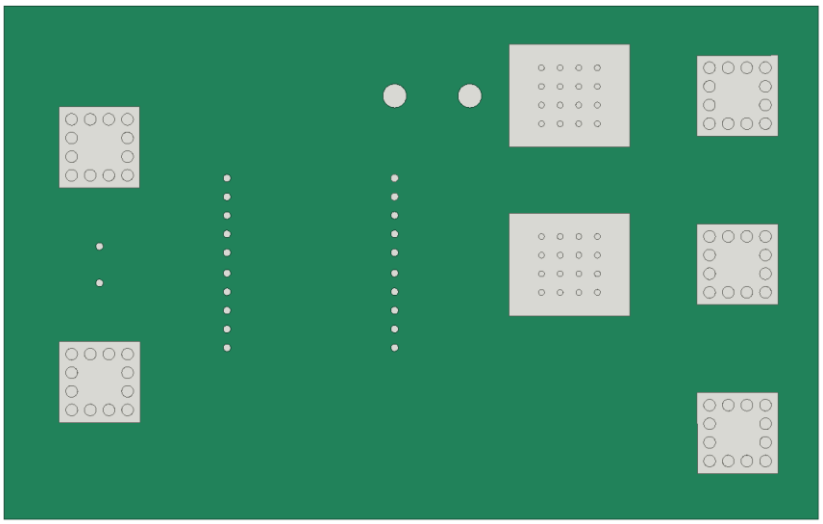


Figure 4-7: Layout #1 bottom side

The 3D geometry model of layout #2 is shown in Figure 4-8. I created it with modifying the model of layout #1, as I did it at the design of the layout, too.

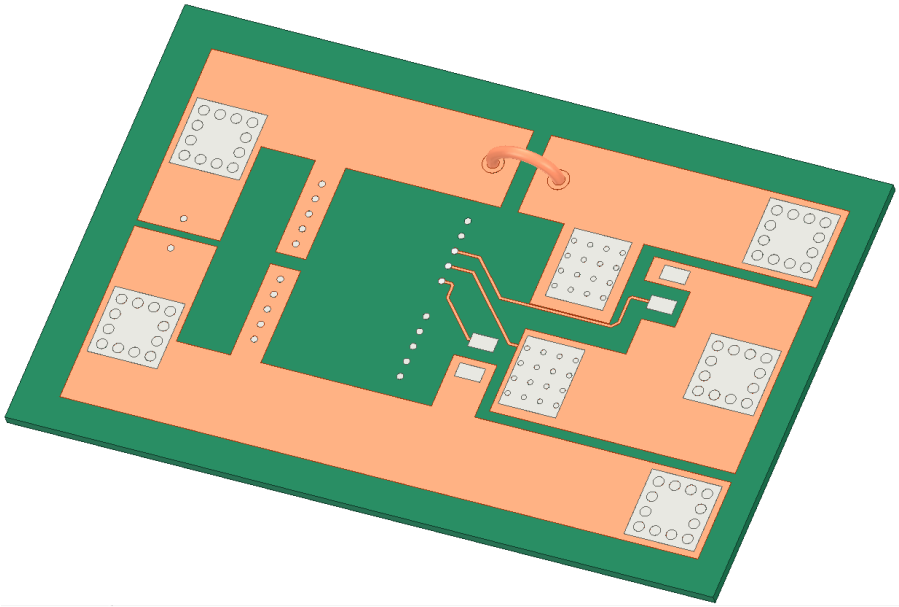


Figure 4-8: 3D geometry model of layout #2

The 3D geometry model of layout #3 is shown in Figure 4-9. Its bottom side is shown in Figure 4-10. I introduce this one because of its parasitic capacitance. Comparing it with Figure 4-9, the sandwich structure (mentioned in 3.3.2) can be seen. I expected that this structure is going to have reducing influence on the induced voltage spikes between different points of the circuit. The measurements confirmed this assumption, as it can be seen in Chapter 7.

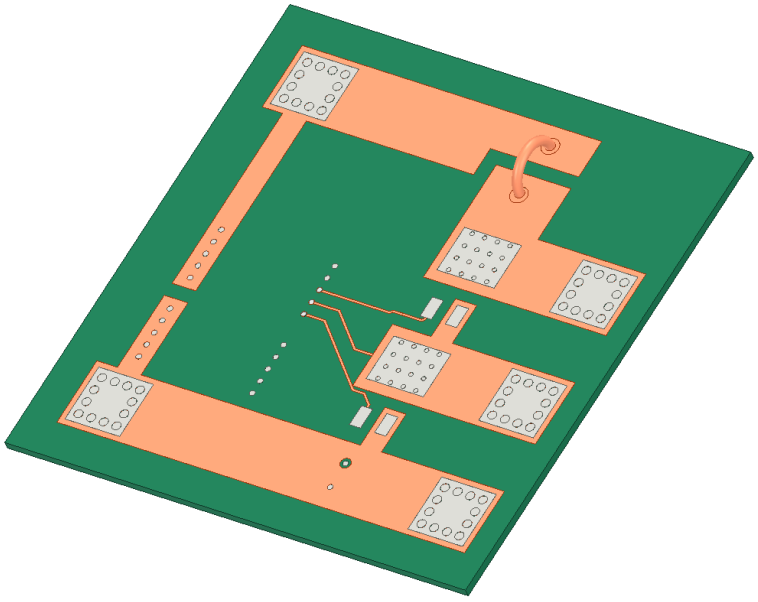


Figure 4-9: 3D geometry model of layout #3

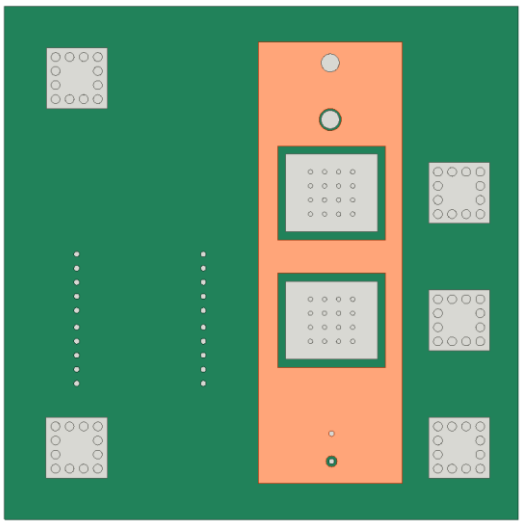


Figure 4-10: Layout #3 bottom side

4.3.3 ANSYS Q3D Extractor

4.3.3.1 Preparations

In this chapter, I am providing a short summary of the preparation procedure of the finite element simulation with ANSYS Q3D Extractor. I overview the required settings, the simulation process and the evaluation of the results.

According to the previous chapter, assume that the 3D geometry model is perfect, and the materials of the components are set properly. If the latter would not be true, it would be impossible to execute the following steps. The next step is generating the nets. A net contains all the conductive objects of the model that are connected to each other in a loop. Whether a material is conductive or not, it can be decided by using the material threshold; if the specific conductivity of the material is over it, it is considered as a conductor, and in the opposite case, it is considered as an insulator. This value can be adjusted manually (the default value is 10 kS/m). For example, a net of layout #1 is shown in Figure 4-11.

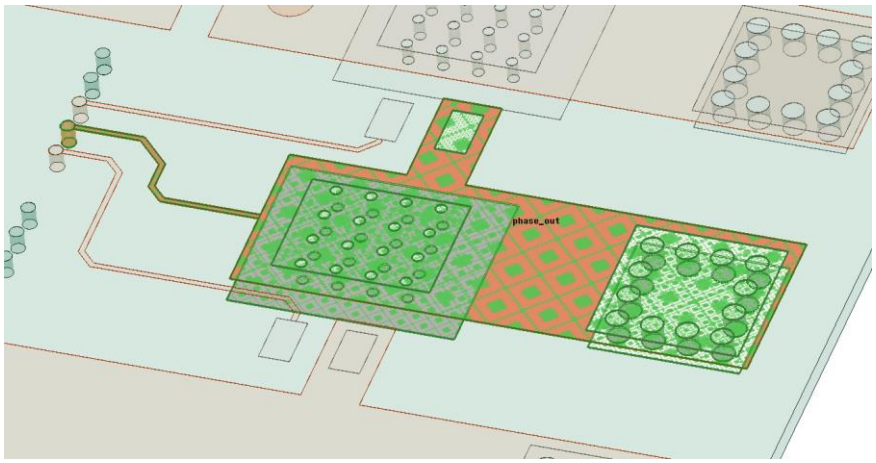


Figure 4-11: One of the nets of layout #1

After generating the nets, source and sink terminals have to be defined to different surfaces of the geometry. These are the specific boundary conditions in Q3D Extractor. A single net can contain multiple sources and a single sink. The output of the simulation is an RLGC model (shown in Figure 4-12) between each source-sink pair that are in the same nets. For example, three sources and the sink of a net in layout #1 are shown in Figure 4-13.

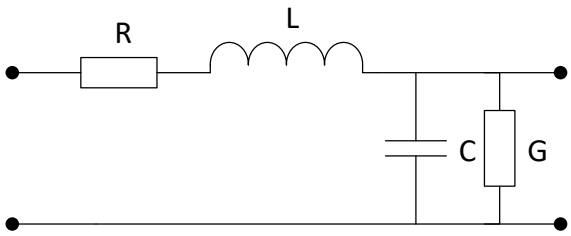


Figure 4-12: RLGC model

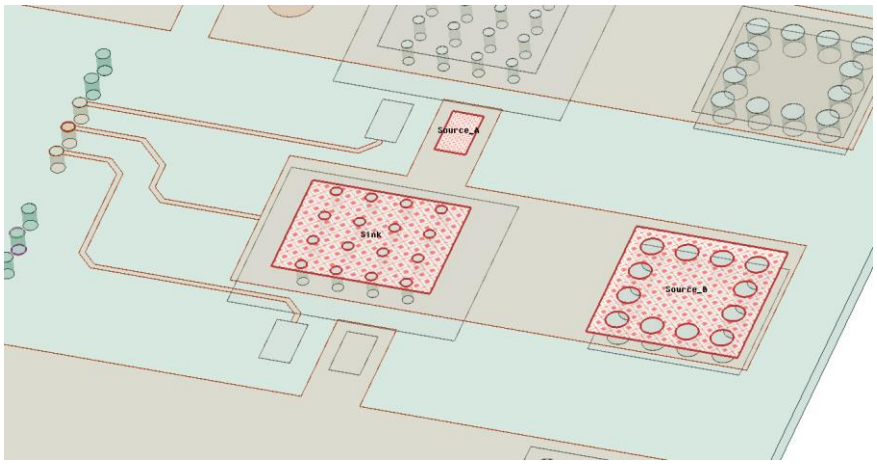


Figure 4-13: Sources and a sink in layout #1

The interpretation of the RLGC models is important part of the work. The results are presented by matrices. The columns and rows are the sources of the nets. The parameters in the main diagonal are the resistance, inductance, capacitance and conductance between the marked source and the sink on the same net. These can be considered as self-resistance, self-inductance, etc. For example, in Figure 4-13, the element in the row and column named ‘Source A’ presents the self-parameters between ‘Source A’ (this is the source pad of the HS MOSFET) and ‘Sink’ (this is the drain pad of the LS MOSFET).

The cells outside the main diagonal are mutual parameters. I neglect these ones in this project, because after checking it, I can say, that they are not significant. An example with explanation for the matrices can be seen below, in Figure 4-18.

After defining sources and sinks to each net, the next step is checking the settings of the finite element mesh. The maximal element size of the mesh, the meshing of objects with curvature etc. can be modified in ‘Mesh operations’ (Figure 4-14), but the process of the mesh generation is automatic in ANSYS Electromagnetics. It means that meshing of every objects is default, and it only changes according to the user’s decision.

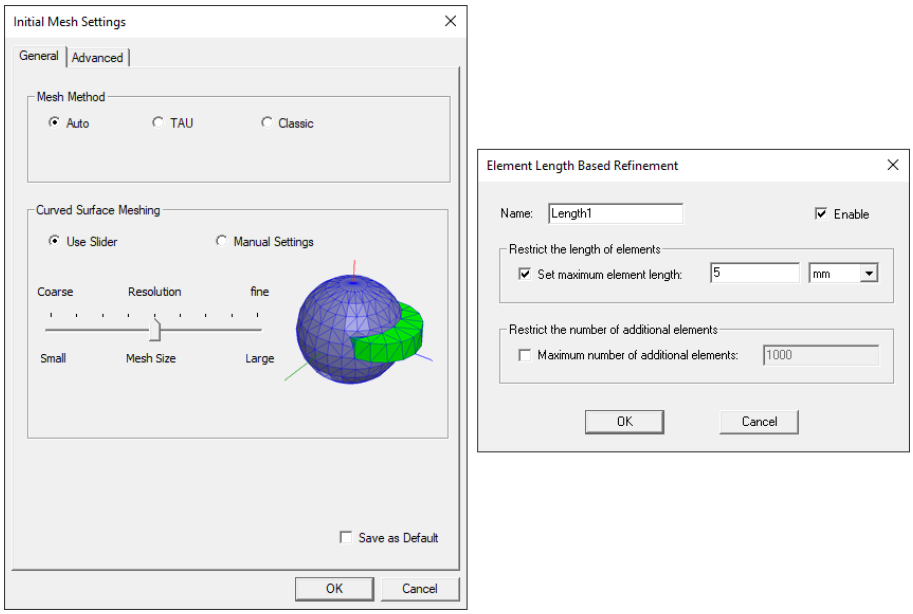


Figure 4-14: Mesh operations

An important preparation step is ‘Analysis setup’ (shown in Figure 4-15). The goals of the simulation can be defined here with ticking the required solution options. A solution frequency can be set here. Remember, that it is a significant disadvantage of the estimation methods, that the frequency dependence can not be handled with them. This problem can be eliminated with FEM. Frequency sweep can also be added to the solution, in this case the RL parameters are counted at each discrete frequency that was set, but the field vectors are only available at the single frequency given here (if ‘Save fields’ is active). The RLGC parameters are contained by separated matrices. The CG (capacitance/conductance)) matrix is frequency independent. The RL (resistance/inductance) matrix has two variants: the DC RL and the AC RL matrices (there are several AC RL matrices, if frequency sweep is required). The user has to define here, whether which matrices’ elements are required to calculate. I only used the RL matrices, because the CG parameters of the PCB wires seemed to be negligible.

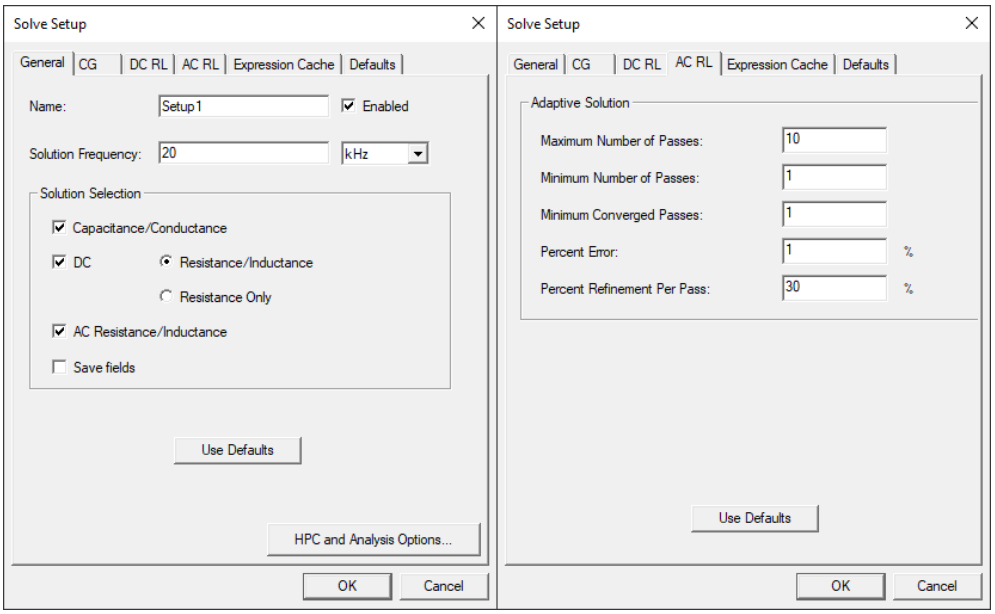


Figure 4-15: Analysis setup

4.3.3.2 Simulation

After setting the analysis options, the simulation can be started. After validating the settings (checking the geometry and supervising, whether everything is set) the software generates the finite element mesh, and calculates the required parameters. In the next step, if the maximum number of passes (in the presented example, 10) is not exceeded yet, it refines the mesh, and calculates the percent error of the parameters compared to the previous step. If the error is over the required value (in the presented example, it is 1%, according to Figure 4-15), it refines the mesh again and so on, until the percent error is under the required value, or the maximum number of refinements is reached. The full procedure's diagram is shown in Figure 4-16.

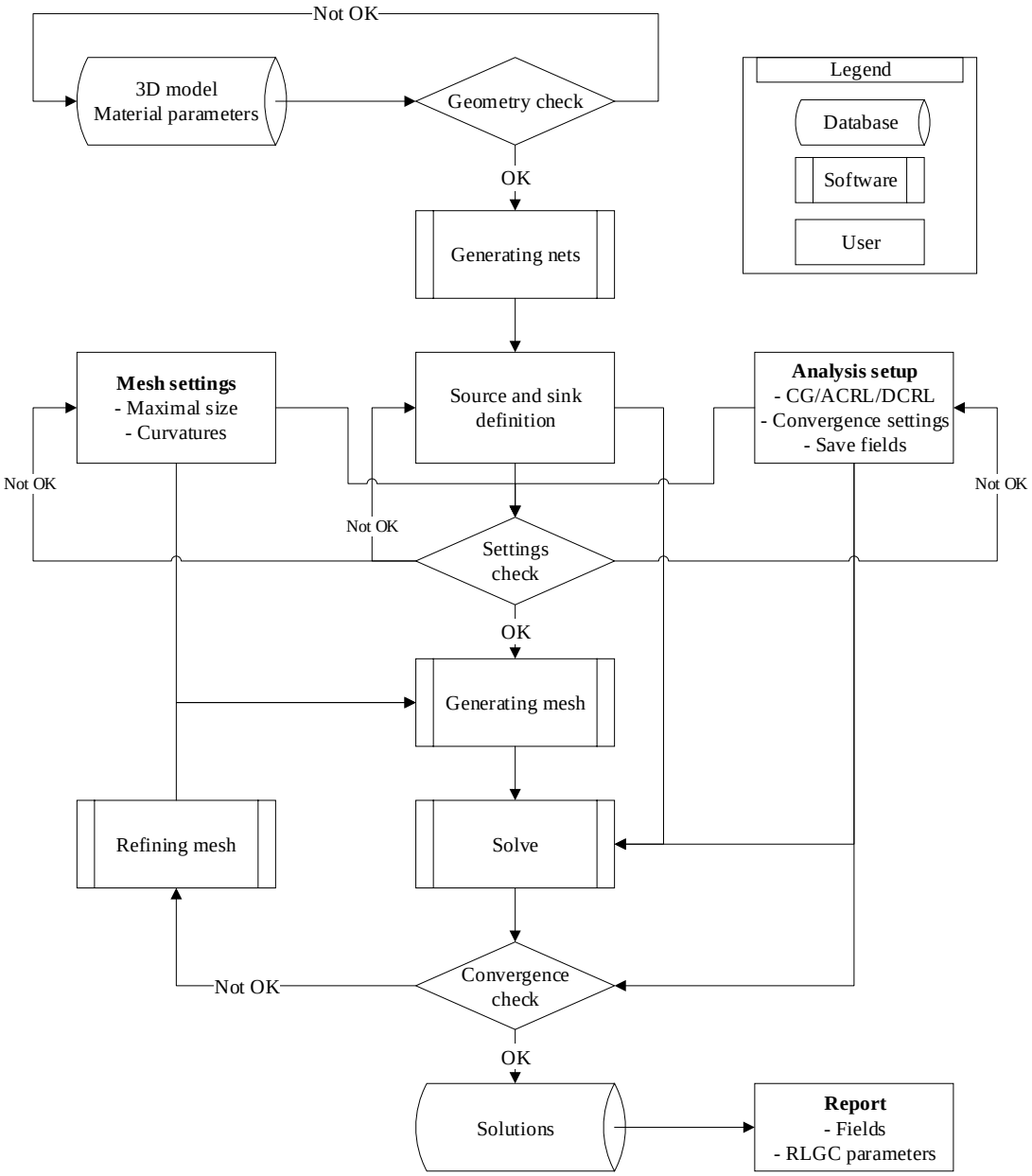


Figure 4-16: Simulation process

The simulation process means the solution of partial differential equations. The software calculates the DC and AC parameters with a different method. Finite element method is applied by calculating the DC parameters. The AC parameters are determined by using the so-called finite volume method (FVM). Briefly, in the FVM the volume integrals containing divergences in the PDEs are converted to surface integrals by using Gauss-Ostrogradsky-theorem. According to this difference between the DC and AC simulations, the DC and AC meshes are also different. An example is shown in Figure 4-17. It can be seen, that the density of the DC mesh is smoother, than the density of the AC mesh, which is stiffer at the margins, due to the skin effect.

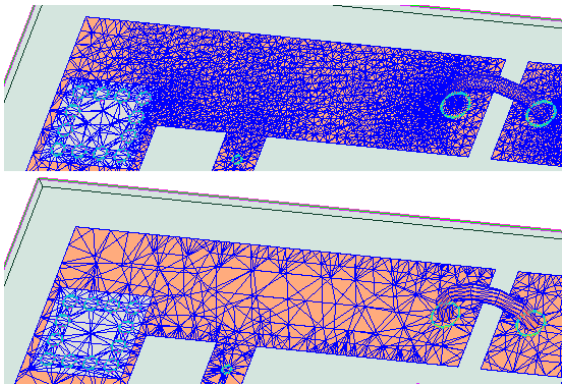


Figure 4-17: Difference between DC and AC mesh

4.3.3.3 Evaluation of results

After reducing the percent error between the results following each other by refining the finite element (or finite volume) mesh, the simulations stops. The last step is evaluation of the results. If overviewing the density of field vectors is a goal, DC and AC field reports can be created, but it is not so common in case of Q3D Extractor. Another module of ANSYS Electromagnetics, Maxwell 3D is appropriate specifically for computing field vectors, and also electrical and magnetic forces due to them. The most important results of the Q3D simulations are the parasitic parameters. As I mentioned above, these are presented by the GC, DC RL and AC RL matrices. An example for AC RL matrix of layout #1 at 20 kHz frequency is shown in Figure 4-18. The rows and columns of the matrix are linked to a source terminal. The elements in the main diagonal are the inductances and resistances between the specific source and the sink of its net. The elements outside the main diagonal are mutual parameters between the conductive paths defined by different sources and the same sink.

Simulation: Setup1 | Sweep1 | DC RL

Design Variation:

Profile | Convergence | Matrix | Mesh Statistics

Resistance Units: mOhm | Matrix | 0 (MHz) | Export...

Inductance Units: nH | Original | All Freqs

Passivity Tolerance: .0001 | Check Passivity | Equivalent Circuit Export...

	ground:Source5	ground:Source6	hsg:Source8	lsg:Source9	phase_out:Source_A	phase_out:Source_B	phase_out:Source_C	vbatt:Source1	vbatt:Source2
Freq: 0 (MHz)									
ground:Source5	2.1877, 7.3025	1.1073, -0.80807	0, -0.75621	0, -1.6654	0, -0.18734	0, 0.79471	0, -0.9543	0, -1.2648	0, 0.38186
ground:Source6	1.1073, -0.80807	5.6901, 37.772	0, 3.5621	0, 4.9125	0, -0.20027	0, -1.7442	0, 3.4192	0, 6.7266	0, -1.2152
hsg:Source8	0, -0.75621	0, 3.5621	50.27, 21.707	0, 3.0105	0, -0.18745	0, -1.0199	0, 4.6852	0, 4.8786	0, -0.89169
lsg:Source9	0, -1.6654	0, 4.9125	0, 3.0105	72.777, 30.015	0, 0.27954	0, -1.039	0, 5.4698	0, 3.2711	0, -0.66382
phase_out:Source_A	0, -0.18734	0, -0.20027	0, -0.18745	0, 0.27954	1.0339, 1.5965	0.0088103, 0.024781	2.0752E-005, 0.11763	0, -0.051206	0, -0.00038171
phase_out:Source_B	0, 0.79471	0, -1.7442	0, -1.0199	0, -1.039	0.0088103, 0.024781	0.86152, 3.3296	3.2708E-007, -0.84156	0, -1.387	0, 0.6252
phase_out:Source_C	0, -0.9543	0, 3.4192	0, 4.6852	0, 5.4698	2.0752E-005, 0.11763	3.2708E-007, -0.84156	44.751, 19.068	0, 3.4767	0, -0.63015
vbatt:Source1	0, -1.2648	0, 6.7266	0, 4.8786	0, 3.2711	0, -0.051206	0, -1.387	0, 3.4767	3.4206, 34.051	6.4098E-007, -1.6946
vbatt:Source2	0, 0.38186	0, -1.2152	0, -0.89169	0, -0.66382	0, -0.00038171	0, 0.6252	0, -0.63015	6.4098E-007, -1.6946	0.85963, 3.3191

Figure 4-18: AC RL matrix example

4.4 Measurement of parasitic parameters

4.4.1 Impedance measurement

In the first part of Chapter 4, I gave an overview of the applied parasitic analysis methods. I started the introduction with the theory of analytical approximations and estimations. In 4.3, I introduced the finite element method and its application briefly, specifically through the example of ANSYS Q3D Extractor.

I analyzed the theoretical possibilities of measuring parasitic parameters, too. Testing these methods was not the goal and part of my work, because I wanted to overview the possible methods of parasitic analysis which are available during the design process.

The largest disadvantage of measurement methods is that these can only be applied, if the designed product is manufactured. In the electrical industry, of course, the analysis has to take place first before the manufacturing. After that, the validation through impedance measurement is available. In this chapter, I mention some methods that are available for this goal.

The parasitic parameters of the electrical circuits appear as parasitic impedance (resistance, inductance and capacitance). Nowadays, even more accurate impedance analyzers are available for measuring them. The simpler ones can only measure at discrete frequencies (these are often mentioned as RLC meters), the more complex ones are capable for frequency sweep, too. My BSc thesis [8] is about impedance measurement, I overviewed the theory of impedance measurement in that.

The impedance measurement process always has two cardinal points of view. The first one is the connection of the measuring instruments to the impedance in focus of the measurement. In case of layout related parasitic effects, it can be seen, that the so-called in-circuit measurement is required, because the parts of the layout can not be separated. The in-circuit measurement requires the connection with at least three wires. Additionally, the connectors also have parasitic effects, and it can influence the measurement. The other important point of view is that the environment also have parasitic effects. To eliminate them, too, the proper connection is via five wires. It is complicated in case of measuring layout related effects.

Measuring of parasitic impedance is often even more complicated. For example, the parasitic inductances usually mean low impedances at low frequencies (in order of

μOhms and mOhms). Low impedance is complicated to measure due to the measurement instruments' and connectors' non-ideality. At high frequencies, where the impedance to measure is higher, the parasitic effects of the environment become more significant, and these make the measurement troublesome.

High-frequency instruments are often used to impedance measurement goals, too. For example, in the mentioned thesis, I overviewed the possibilities of impedance measurement with a network analyzer. It is appropriate for measuring transfer functions of linear systems fundamentally, but it can be used for impedance measurement, too. Its two ports (the Gain-Phase port, which is for measuring transfer function between input and output voltages, and the S-port, which is dedicated to measure scattering parameters) are appropriate for that. The main problem in case of them are also the connectors non-ideality, and the parasitic effects of the environment, that have to be eliminated.

The examples mentioned highlight that several troubles can come forward in case of measuring parasitic impedance. To get a comprehensive overview, and choose the best method(s), every ones should be analyzed with full particulars, but it is not the goal of this project.

4.4.2 Indirect measurement

In the previous chapter, I mentioned some impedance measurement methods to determine layout related parasitic effects. In this chapter, I introduce a well-tried method for estimating the inductance of conductive paths with measurements that are not based on impedance analysis.

When the current of an inductor changes, induced voltage appears between the terminals of the device, according to Equation 1-2, mentioned in Chapter 1. According to Lenz's law, the direction of the induced voltage (or current) is such, that it generates a magnetic field that reduces the effect producing it. It means that the direction of the current changing and the voltage changing is opposite. This effect can be observed through measurements. Theoretically, the inductance of the conductive path can be derived as the ratio of the peak value of the voltage inducing in it, and the gradient of the current.

$$L = \left| \frac{\hat{V}_{ind}}{\frac{di}{dt}} \right|$$

Equation 4-21: Calculating inductance

Equation 4-21 is only valid if the change of the current is linear. This assumption usually is not true in the whole period of the changing. The gradient, and so the inductance can be estimated with the ratio of the linear current change and its time.

$$L \cong \left| \frac{\hat{V}_{ind}}{\frac{\Delta I}{\Delta t}} \right|$$

Equation 4-22: Estimation of inductance

This indirect measurement method based on measuring voltage and current is appropriate to estimate the inductance of conductive paths. I am introducing it through an example in Chapter 7.

Theoretically, the measurement of resistances of the conductive paths is also possible indirectly. In this case, the voltages and currents have to be measured in steady state. The ratio of the voltage difference between two points and the current flowing in direction of either to the other one presents the resistance of the section. In case of layout related parasitic resistances, this method is not appropriate, because these resistances are in order of mOhms, and attainably accurate instruments would be needed to measure the voltage drop on them.

5 Parasitic analysis of the designed circuits

5.1 Electrical circuit models

In the previous chapters, I overviewed some methods that could be used analyze the layout related parasitic effects. The design process of the circuits was also presented. In this chapter, I introduce the parasitic analysis of the circuits with the methods mentioned. I use layout #1 as a demonstration example. The process of parasitic analysis is similar in case of the other ones, too.

The goal is to create the electrical model of the three different circuits containing the layout related parasitic effects. The critical parameters are resistance and inductance, so I use lumped element RL two-poles. The parasitic model of layout #1 is shown in Figure 5-1. It can be seen, that the model of the power supply, the Ecap, the bridge driver board and the load are not parts of the layout's parasitic model.

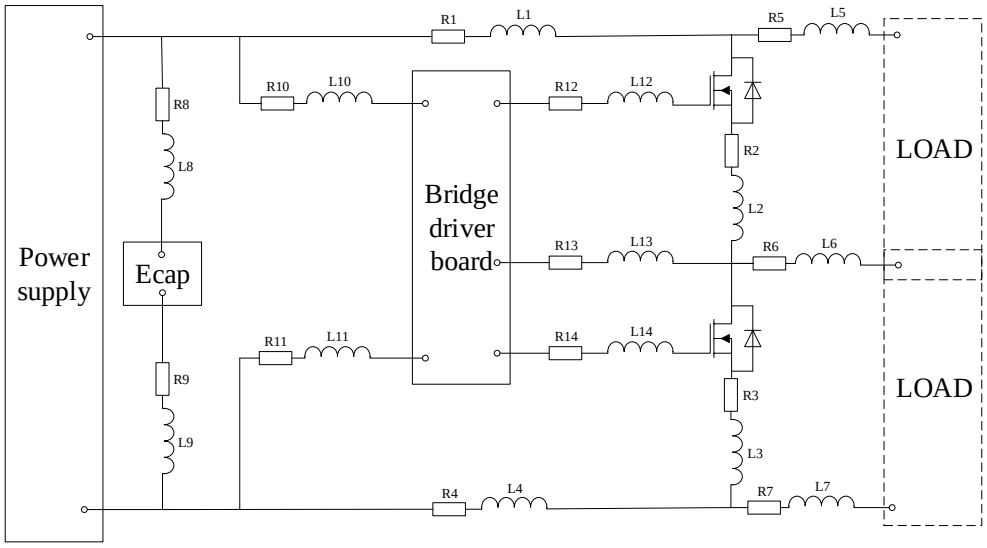


Figure 5-1: Parasitic model of layout #1

This circuit contains 14 different series RL two-poles, which are presented in Table 5-1. Let's overview this model in aspect of reduction.

$RL_{5\text{-}7}$ can be neglected, because the inductances and resistances of these two-poles are lower at least with two or three orders of magnitude than the load's inductance and resistance. $RL_{10\text{-}11}$ are also negligible, because these ones model the supply wires of the bridge driver IC that have no influence on the switching process. $RL_{12\text{-}14}$ are the wires connecting the driver with the gate electrodes of the MOSFETs and with the phase output point. The inductance and resistance of these wires can influence the switching times

theoretically, but due to their low values (in order of 10 mΩ and 10 nH), the influence is not significant.

The remaining ones, $RL_{1\text{-}4}$ and $RL_{8\text{-}9}$ are important in aspect of the switching process, because they directly influence the transient phenomenon. These ones definitely have to be parts of the model. I note that I did not neglect the elements mentioned in the previous paragraph. It would only be advantageous, if I would like to calculate parameters manually, not by simulation.

The process of creating models is similar in case of the other two layout variants. The models can be seen in the Chapter 'Parasitic models' of the Appendix.

#	Current	Properties
1	High	Directly influence the switching transients. Definitely have to be the parts of the electrical model.
2	High	
3	High	
4	High	
8	High	
9	High	
5	High	Can be neglected because of the low values compare to the load's parameters.
6	High	
7	High	
10	Low (Supply)	Can be neglected because of no influence on the switching procedure.
11	Low (Supply)	
12	Low (Drive)	Can be neglected because of low influence on the switching procedure.
13	Low (Drive)	
14	Low (Drive)	

Table 5-1: Elements of layout #1's parasitic model

In the next chapters, I introduce the derivation of the parasitic model's parameters with the methods mentioned in Chapter 4.

5.2 Analytical approximations, estimations

5.2.1 Separating the coherent, polygon-shaped conductive paths

According to Chapter 4.2, I created the parasitic models of the designed circuits firstly with approximations. To calculate DC resistance and inductance, I used the rule of thumb method, and the equations mentioned in Chapters 4.2.1 and 4.2.2. The formulas assume constant cross-section area. To ensure it, I segmented the coherent, polygon-shaped conductive paths to rectangular-shaped ones. Figure 5-2 shows the segmentation of the paths of layout #1. Segments #1 and #3-14 are rectangular-shaped ones with the thickness of 18μm. Segment #2 is the piece of wire mentioned in Chapter 3.3.1, that is

possible to solder into the PCB to connect the conductive paths. It has a curve, but in case of these estimations, it is assumed that this piece of wire is straight. Segments #15-17 are assumed to be straight also.

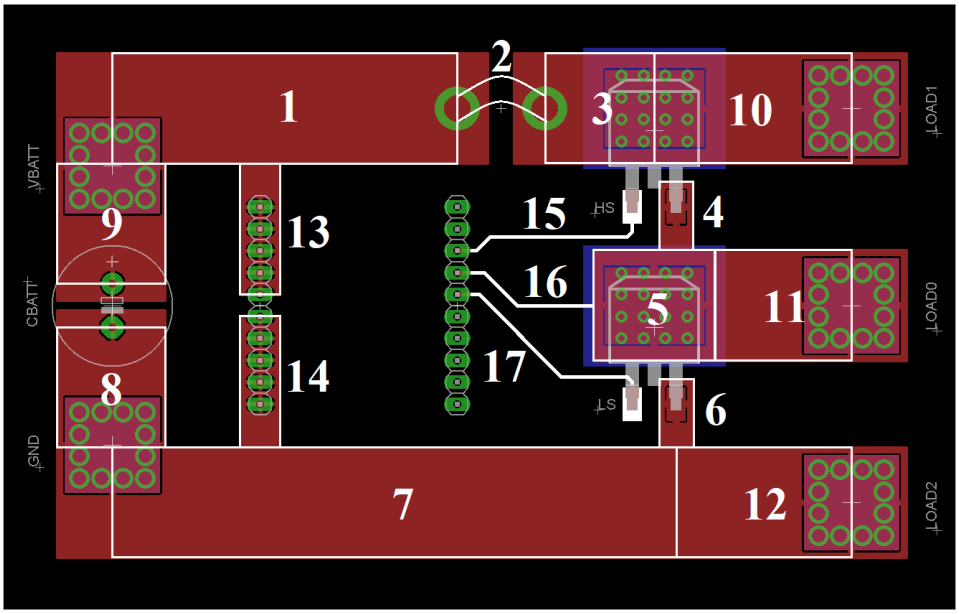


Figure 5-2: Rectangular-shaped segments of layout #1

The segmentation of layout #2 and #3 can be found in Chapter 'Rectangular-shaped segmentation and parameters' of the Appendix.

5.2.2 Rule of thumb: '$1\ mm = 1\ nH$'

The '$1\ mm = 1\ nH$' rule of thumb introduced in Chapter 4.2.2.4 presents a simple estimation of inductance. According to it, in this case, only the lengths of the conductive segments are required to get the value of their inductance. For example, the length of segment #1 of layout #1 is 40 mm. According to the rule of thumb, its inductance is approximately 40 nH. After deriving the inductance of every segments this way, I determined the parameters of the parasitic model (shown in Figure 5-1). For example, the inductance L_1 contains the inductances of segments #1-3: $L_1 = 40 + 32 + 13 = 85\ nH$, and so on. The resistances of the parasitic model were calculated with the formulas of DC resistance, presented in Chapter 4.2.1.1.

5.2.3 Approximation with analytical formulas

The explicit, analytical formulas linked in Chapter 5.2.1 require all the geometrical parameters of the conductive segments. In case of rectangular cross-section, the length, width and the thickness is required. In case of the piece of cylindrical wire, its

length and radius is required to calculate its inductance (and resistance also). The assumption is that DC current flows through the conductive segments, with homogenous density through their volume. The results can be found in Chapter 'Rectangular-shaped segmentation and parameters' of the Appendix.

This method and the previously mentioned rule of thumb are only capable for coarse estimations. Its first reason is that there is no exact method to segment the conductive paths. The method I used is one of the possible solutions, and is only an approximation. Another reason is the nonlinearity of the formulas used to calculate the inductances of the parasitic model (presented in Chapter 4.2.2.2). Additionally, the geometry limits of the formulas do not come true in case of every segments. For example, segment #8-9 are almost square-shaped segments. For these, $l > w$ stands, but $l \gg w$ does not stand, so theoretically, none of the inductance formulas are allowed to use in case of them.

I would like to highlight that as it can be seen, the last two methods have conceptual obstacles, but these are even so commonly used (incorrectly), if the finite element method is not available. The difference is going to be presented in Chapter 8.

5.3 Finite element method

5.3.1 Preparations and settings of the simulations

In Chapter 4.3, I presented the FEM briefly. In this chapter, I introduce the process of the analysis with it, through the example of layout #1. After creating the 3D geometry model of the circuit and setting the materials, I gave the required settings. The nets are generated automatically. These are shown in Figure 5-3.

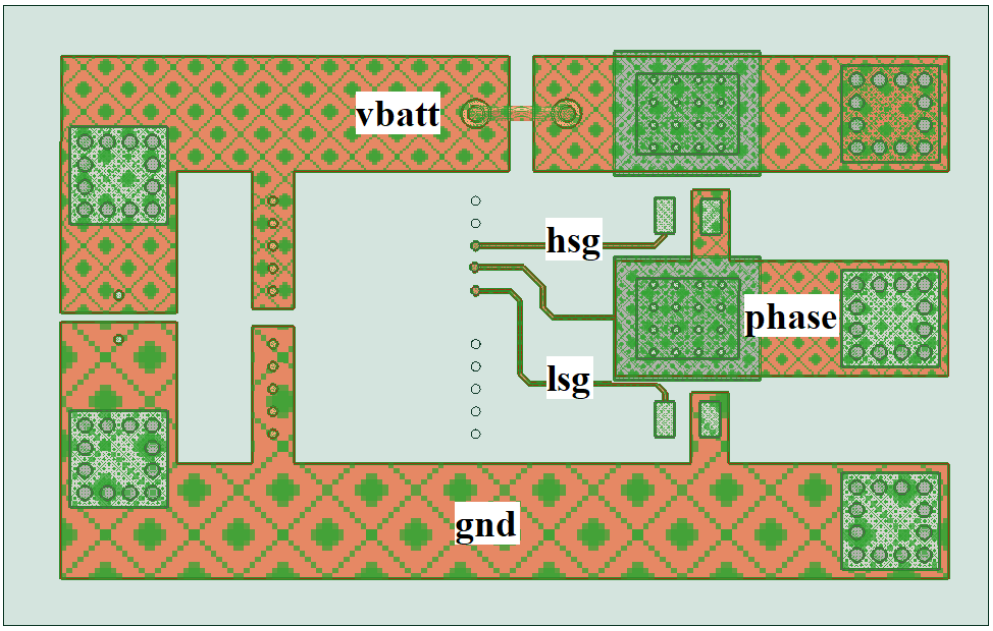


Figure 5-3: Nets of layout #1

After generating the nets, I defined the excitations. These are shown in Figure 5-4. It is important to consider, that every net have to contain exactly one sink, and one or multiple sources. The results are the RL parameters between the sources and the sink of the specific net (the CG, and all the mutual parameters are neglected, as I mentioned earlier).

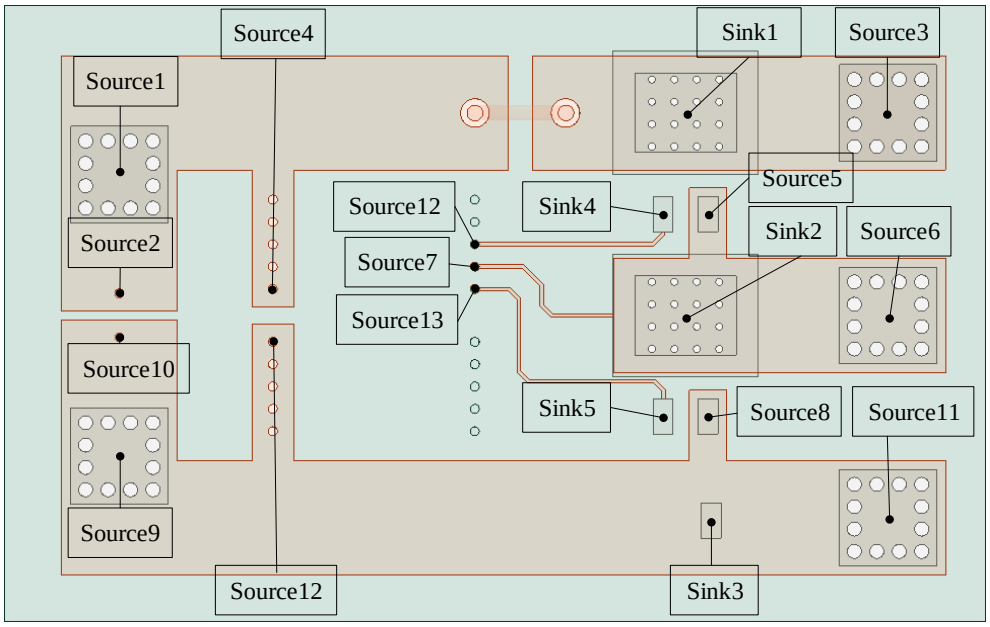


Figure 5-4: Excitations of layout #1

I set the maximum length of the finite elements to 10 mm. The solution frequency is 20 kHz (this is the switching frequency of the circuit). The RL parameters are also

derived at 0 Hz (DC RL). The model parameters derived by the finite element analysis can be found in Chapter ‘Parasitic models’ of the Appendix.

5.4 Summary

In the previous chapters, I presented the parasitic analysis methods I tried through the example of layout #1. Figure 5-5 shows the diagram of my project. After designing the circuits, I executed the analysis with estimations, approximations and finite element analysis. I used the RL parameters derived by different methods as input of electrical simulations (introduced in Chapter 6). The outputs of these simulations are the characteristics of the switching transients. The analyzed parameters are the peak values and the ringing frequencies of the induced voltages between different points of the circuits.

In Chapter 7, I am introducing the measurements. My goal was to investigate the same moments of the switching process, as in case of the electrical simulations based on the parasitic parameters. The final goal was to compare the measured characteristics to the simulated ones, and choose the parasitic analysis method, which one(s) provided the best models of the circuits. I present the comparison in Chapter 8.

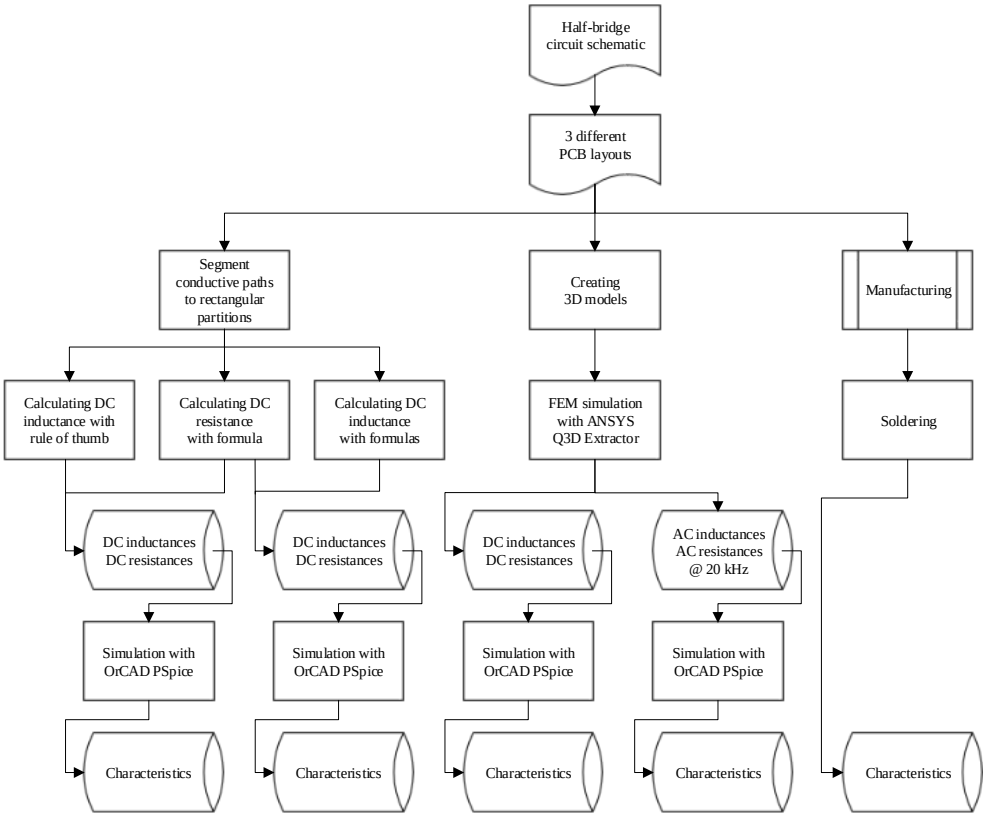


Figure 5-5: Parasitic analysis methods

6 Electrical simulations

The parasitic analysis methods provided the parameters of the model circuits of the three different layouts. The models and the parameters are included in the tables of Chapter 'Parasitic models' of the Appendix. I complemented the model circuits with the models of the power supply, the Ecap, the bridge driver IC, the MOSFETs and the load.

The power supply I used is implemented as an ideal voltage source. I used 12 V supply voltage. It is proper for the MOSFETs, and also for the driver IC. The maximum value of the current was about 15 Amps. It is determined by the resistance of the load, because it is higher with two orders of magnitude, than the resistance of the layout's conductive paths. The parameters of the wires connecting the power supply with the board were determined by measurement with an RLC meter. The inductance of these wires and the Ecap are realizing a low-pass filter that eliminates the bouncing of the power supply.

As I mentioned in Chapter 3.4.1, I realized the load by connecting wire wound resistors parallel. It resulted a resistive load with the resistance of 750 mΩ and the inductance of 1.5 μH. I measured these values with an RLC meter. These parameters do not have to be determined with high accuracy, because they do not influence the induced voltages primarily. The only important point of view was to choose the value of the resistance low enough to ensure relatively high current to escalate the amplitudes of the induced voltages spikes.

The Ecap's model contains its nominal capacitance (1000 μF) and its ESR, which is 110 mΩ according to its datasheet. The ESL is often estimated with the frequently mentioned rule of thumb. Its inductance in nH can be approximated with the distance of its leads in millimeter (5 mm → 5 nH).

The Onsemi NCP5111 bridge-driver IC and the power MOSFET I used have an online available model that can be downloaded from the manufacturers' webpage. I used these ones in the simulation models. The circuits, which are containing the parasitic parameters related to the layouts and the devices mentioned above were built in ORCAD Capture. I performed the simulations with ORCAD PSpice A/D.

The model of layout #1 based on the ACRL parameters derived by finite element analysis is shown in Figure 6-1. The models of the other two layouts can be found in Chapter 'Electrical simulation models' of the Appendix.

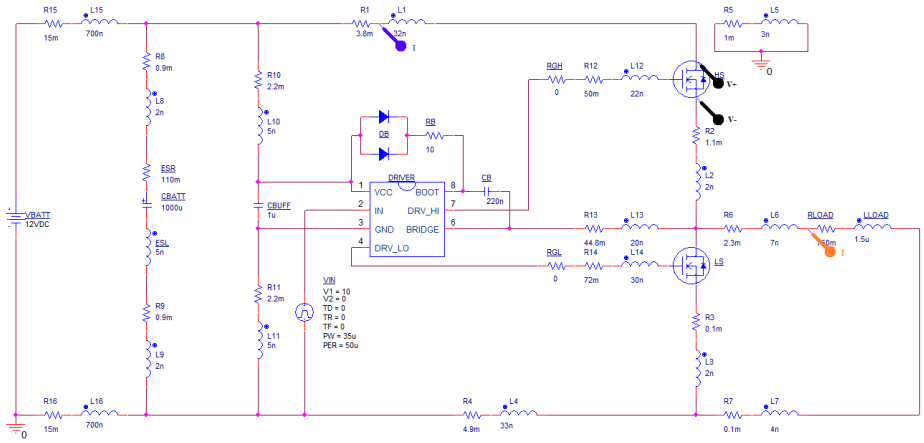


Figure 6-1: Electrical model of layout #1 with simulated ACRL parameters

A simulation example is shown in Figure 6-2. The currents and the HS D-S voltage are ‘measured’ with current probes, and a differential voltage probe, like in case of the measurements, too. The ringing frequency is 12 MHz, and the peak value of the D-S voltage is 43.9 V. The induced voltage is 31.9 V.

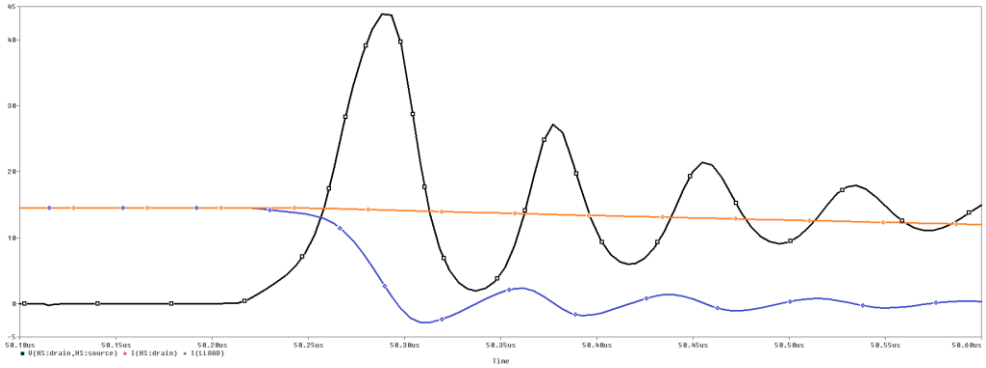


Figure 6-2: Simulated characteristics

I observed the differential voltages between different points (presented in the next chapter) of the circuits, and saved the characteristics. The goal was to compare them with the measured values.

7 Measurements

7.1 Measurement of induced voltage characteristics

In this chapter, I am introducing the measurements. My goal was to measure the characteristics of the switching transients, and compare them with the simulation results. The measurement setup and the devices I used can be seen in Chapter ‘Measurement setup’ of the Appendix. The block diagrams of the measurements of layout #1 are shown in Figure 7-1 and Figure 7-2. I performed the measurements with connecting the load between the phase output point and the ground, and between the phase output point and the battery also.

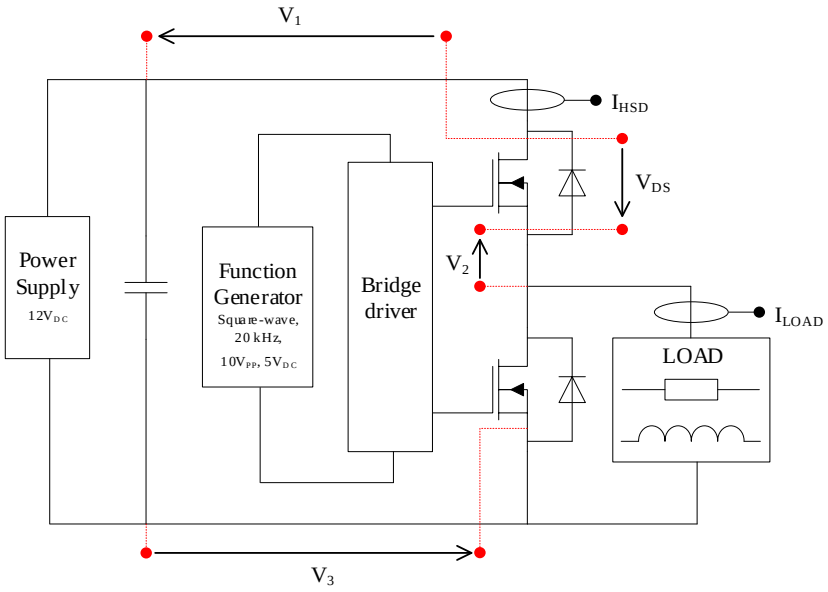


Figure 7-1: Measurement block diagram 1

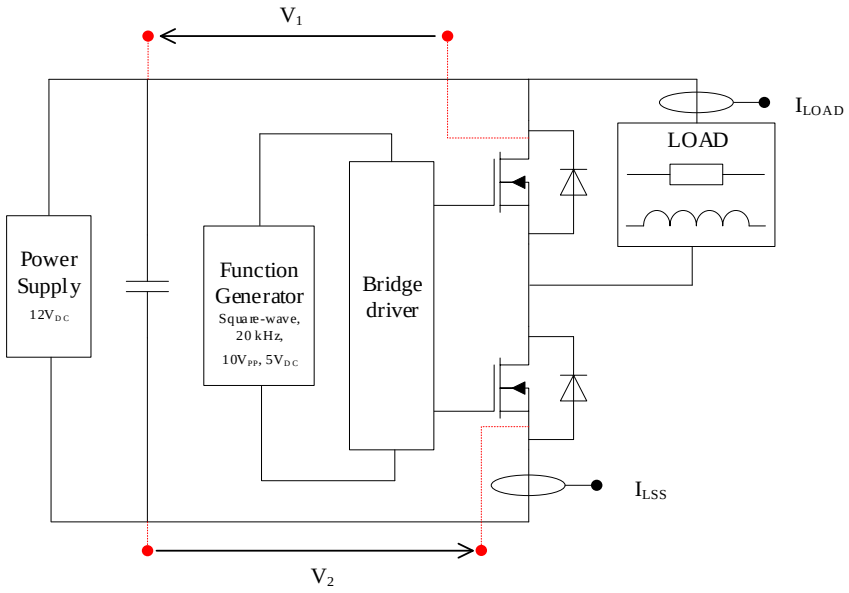


Figure 7-2: Measurement block diagram 2

I measured the currents with Rogowski coils [9], and observed the signals with an oscilloscope to catch the moment of switching. The Rogowski coil is a current transformer, and is capable for measuring AC signals. Its advantage is the small size. For example, it is possible to measure the source current of MOSFETs, as it is shown in Figure 7-3. It is also possible in case of the used D2PAK MOSFETs, there is enough place under the pins for the wire.

Figure 7-3: Rogowski coil [9]

The induced voltages in the moment of switching were measured by a differential probe between different points of the circuit. The points are shown in Figure 7-1 and Figure 7-2 in case of layout #1. An example is shown in Figure 7-4. In this case, the load was connected between the phase output point and the ground. I observed the induced voltage between the drain and the source of the HS MOSFET in the moment of switching. When the device switches off, its current (blue) decreases to zero after a short ringing. After the switching, the voltage of the phase output point has to be approximately equal

to the supply voltage. Due to the current's cutting off and the inductances of the system, induced voltage spike appears between drain and source, and the final value is getting reached after oscillation. The peak value and the frequency of this signal are the important parameters. In this case, the frequency is 12.4 MHz, the induced voltage is 22 V (it is measured by cursors in the figure), and the peak value of the D-S voltage is 34 V.

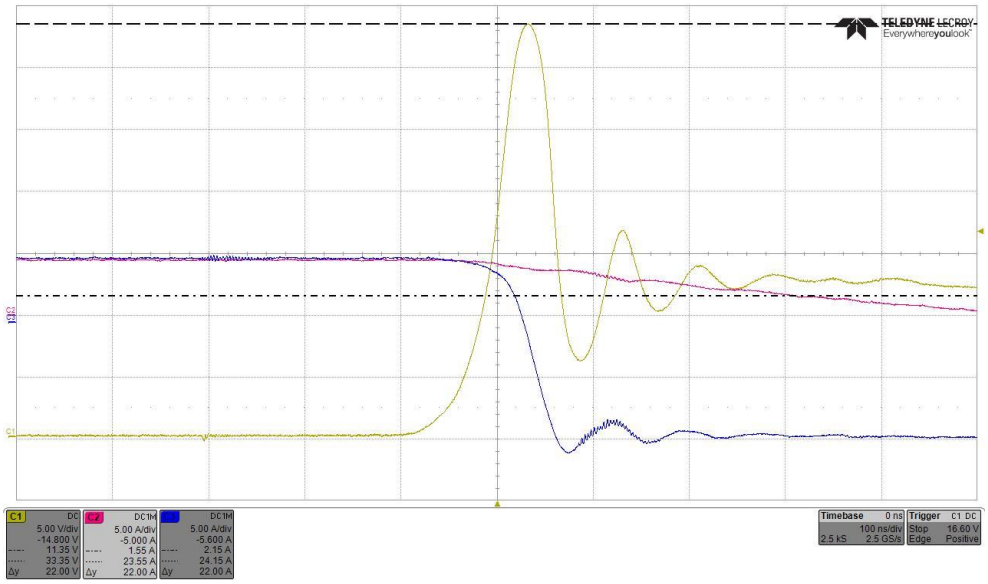


Figure 7-4: Measured characteristics

This example presents the same case, as the example of Chapter 6 (Figure 6-2). It can be seen, that the parameters are approximately equal.

7.2 Indirect measurement to estimate inductance

In Chapter 4.4.2, I introduced the estimation of inductance through voltage and current measurements. In this chapter, I demonstrate this method through an example. The measurement setup is shown in Figure 7-5. The measured differential voltage is between HS drain and the connecting point of the power supply. Thus, the inductance of this conductive path is estimated.

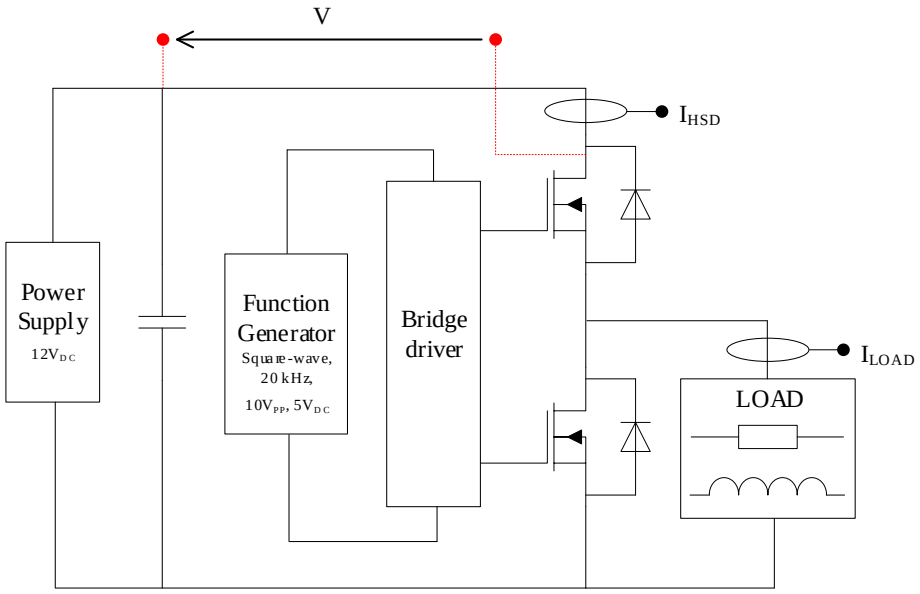


Figure 7-5: Indirect inductance measurement

The measured characteristics are shown in Figure 7-6. As I mentioned earlier, the gradient of the current have to be calculated in the linear section. The most appropriate solution is to save the measured data, investigate the linear section, and calculate the gradient by software.

An estimation is shown in Figure 7-6, according to Equation 4-22.

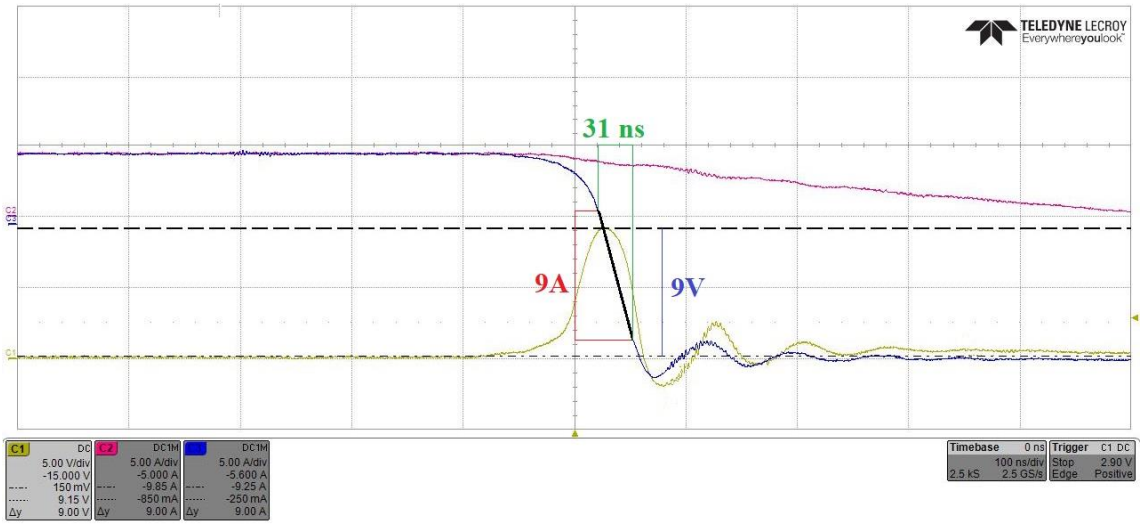


Figure 7-6: Inductance estimation

The estimated inductance can be calculated as

$$L \cong \frac{\hat{V}_{ind}}{\left|\frac{\Delta I}{\Delta t}\right|} = \frac{9\ V}{\frac{9\ A}{31\ ns}} = 31\ nH$$

Table 7-1 shows the values derived in Chapter 5 for this conductive path.

Rule of thumb	Formula	DC simulation	AC simulation	Measurement
85 nH	42 nH	35 nH	32 nH	31 nH

Table 7-1: Inductance of RL_1

It can be seen, that the result converges to the values derived by the FEM simulations. According to my experiences, the best models of the circuits are based on these methods (see in Chapter 8). It can be seen, that this kind of estimation of inductance is an appropriate method to use.

8 Conclusions

8.1 Goals

In this project, I analyzed some methods for modelling layout related parasitic effects. To demonstrate these ones, I designed half-bridge circuits with three different topologies. I performed the parasitic analysis with the methods learned, and I used the results as input of electrical simulations. After manufacturing the PCBs, I measured the same quantities which I investigated with the simulations. In this chapter, I am going to present the results, and the classification of the methods used for parasitic analysis.

8.2 Results

The most important parameter is the ringing frequency of the induced voltages appearing between different points of the circuits. Thomson's formula for the resonant frequency is presented by Equation 8-1.

$$f = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{LC}}$$

Equation 8-1: Thomson's formula

I measured differential induced voltages in case of every layout, connecting the load in two different ways. The measurement results and the simulation results are shown in Table 8-1. It is perceptible, that the frequencies resulted by the simulations are lower in every case, than the measured ones. According to Thomson's formula, it means, that an upper limit is provided for the inductances.

The measurement of layout #1 with connecting the load between the phase output and the ground, is shown in Figure 8-1.

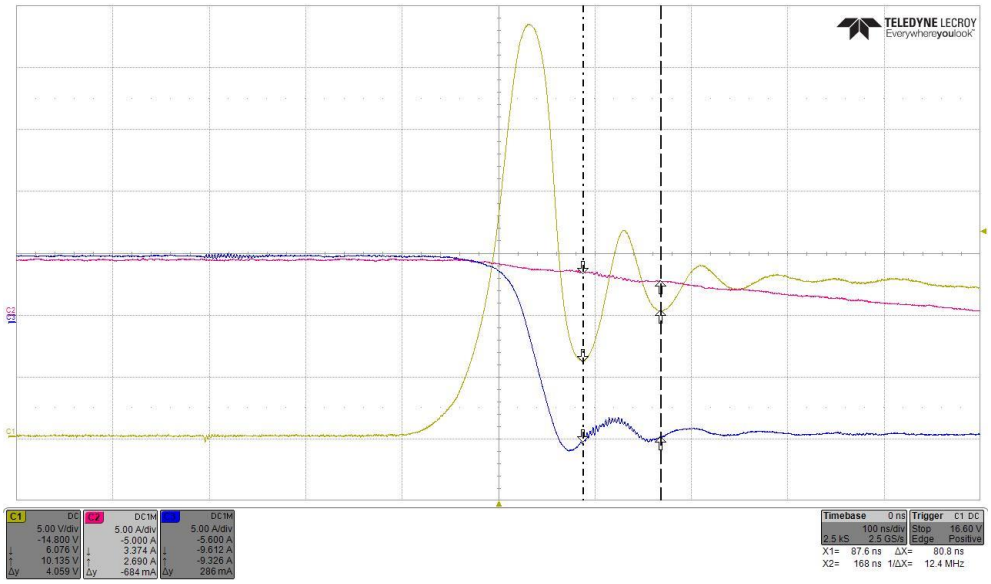


Figure 8-1: Measurement of ringing frequency

Layout	1		2		3	
Load	LS	HS	LS	HS	LS	HS
Measurement	12.4	12.4	12.4	12.8	18	19
Rule of thumb	7.8	7.9	7.6	7.8	9.9	10.1
Formulas	9.7	9.9	10	10.1	11.1	11.2
DC simulation	11.9	12	11.9	12.4	16.6	17.3
AC simulation	12	11.9	12	12.5	16.6	17.4

Table 8-1: Ringing frequencies of induced voltages [MHz]

The percent errors are shown in Figure 8-2. The reference is the measurement, because the goal is to model the real operation of the circuits.

The estimation methods (the rule of thumb and the analytical approximation) did not provide a proper model of the circuits, as it can be seen in the diagram. These results highlight that the use of these methods should be avoided according to the conceptual obstacles introduced in the previous chapters.

The percent errors are under 10% in case of the FEM simulations. It means, that these methods provided proper models. It is not unambiguous, whether the DC or the AC simulations are better. Its reason is that the 20 kHz frequency is not high enough to escalate the difference between these ones. The conclusion is that in this frequency range the two methods provide approximately equivalent results.

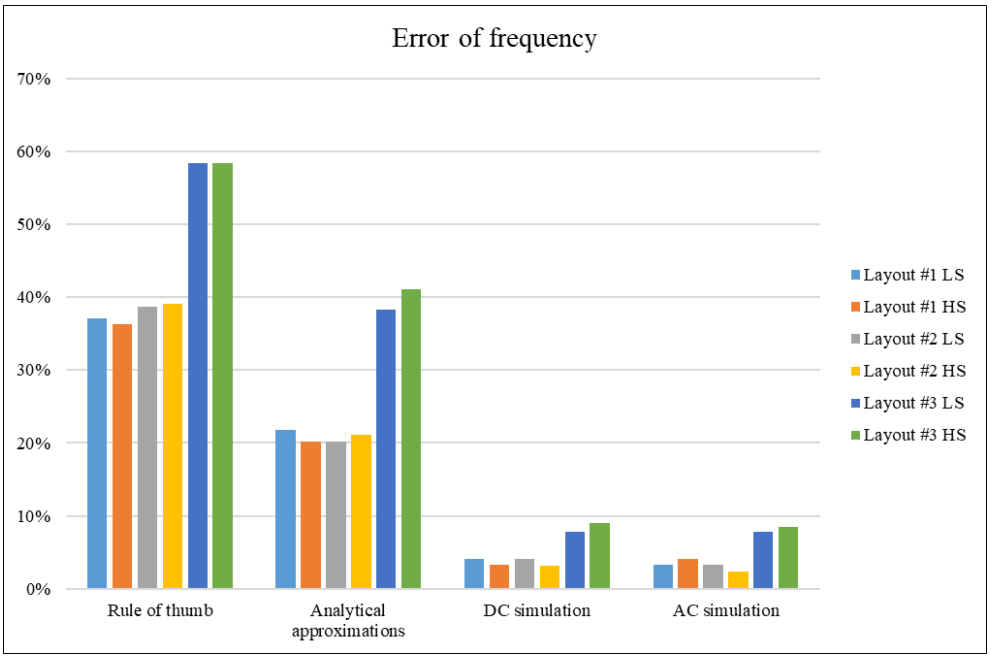


Figure 8-2: Error of frequency

It is important to highlight that the frequency errors of layout #1-2 are under 5%, which is a valuable consequence. This value is higher in case of layout #3. It means that the model of this layout is not as proper as the others'. Its reason is the sandwich structure mentioned in Chapter 3.3.2. Due to the capacitance appearing between the conductive paths on the top and the bottom side of the PCB, the inductance of the loop created by the MOSFETs decreases 'virtually', and it causes the increasing of the ringing frequency, according to Thomson's formula (Equation 8-1).

Hereinafter, I deal only with the models presented by the FEM simulations, because the other ones did not provide proper models of the circuits, and so there is no point to analyze them anymore.

According to the experiences presented thus far, it is presumable that the modelling provides usable results. The other important parameters to observe are the peak values of the induced voltages. The most important goal was to determine, whether how exactly the real operation can be modeled. I expected preliminarily that the simulations are going to provide higher values, than the measurements, because the attenuation caused by the measurement environment is not implemented in the parasitic models. I also assumed that in case of lower induced voltages (and so conductive paths with lower inductance) the modelling is going to provide higher inaccuracy, because the lower the parasitic effect is, the more difficult it is to observe it.

The results can be found in Chapter ‘Measurement results’ of the Appendix. Comparing the above mentioned simulation and measurement example (Figure 6-2 and Figure 7-4), it can be seen that the amplitude of the D-S voltage is lower in case of the measurement, and the damping of it is faster. This is not only true in case of the presented D-S voltage, but also in case of every differential induced voltages. Thus, my first assumption is verified.

The absolute error of the measured differential voltages of layout #1 are shown in Figure 8-3. My second assumption was also correct, because the higher the measured voltages are, the lower the error is. The D-S voltages are estimated with approximately 25% error. According to that, every single nanohenries can influence the induced voltages; this is a valuable consequence. The difference between the models provided by DC and AC FEM simulations are not significant from this point of view.

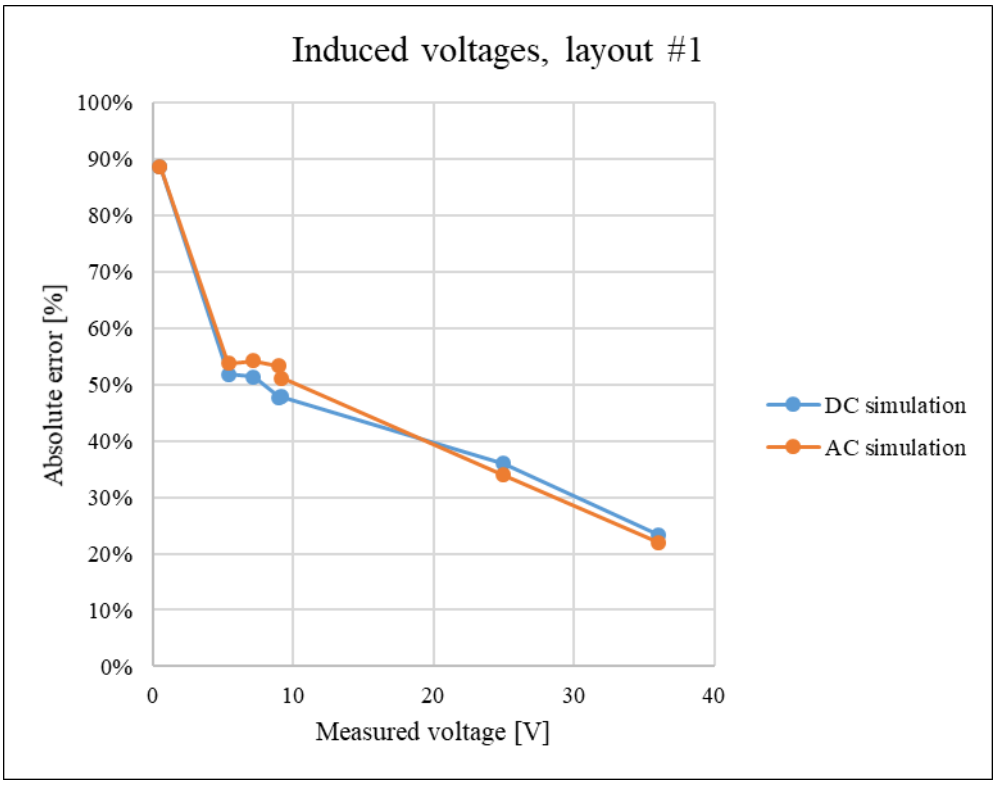


Figure 8-3: Induced voltage estimation error, layout #1

The tendency is the same in case of layout #2 (shown in Figure 8-4).

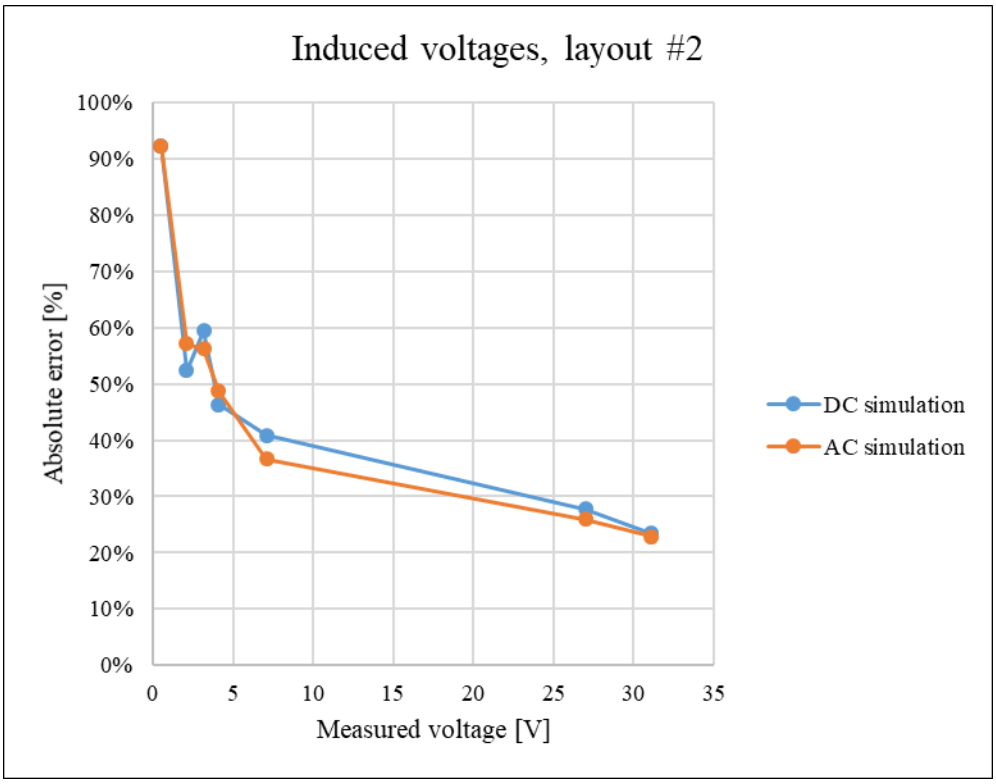


Figure 8-4: Induced voltage estimation error, layout #2

Let's analyze the results of layout #3, shown in Figure 8-5. Due to the sandwich structure, the amplitudes of the induced voltages are decreased. All the measured differential voltages (except the D-S voltages) are under 5 Volts. It is the either reason, why the errors are higher, than in case of the other two layouts. The other reason is that the model is not perfect, and it also increases the error.

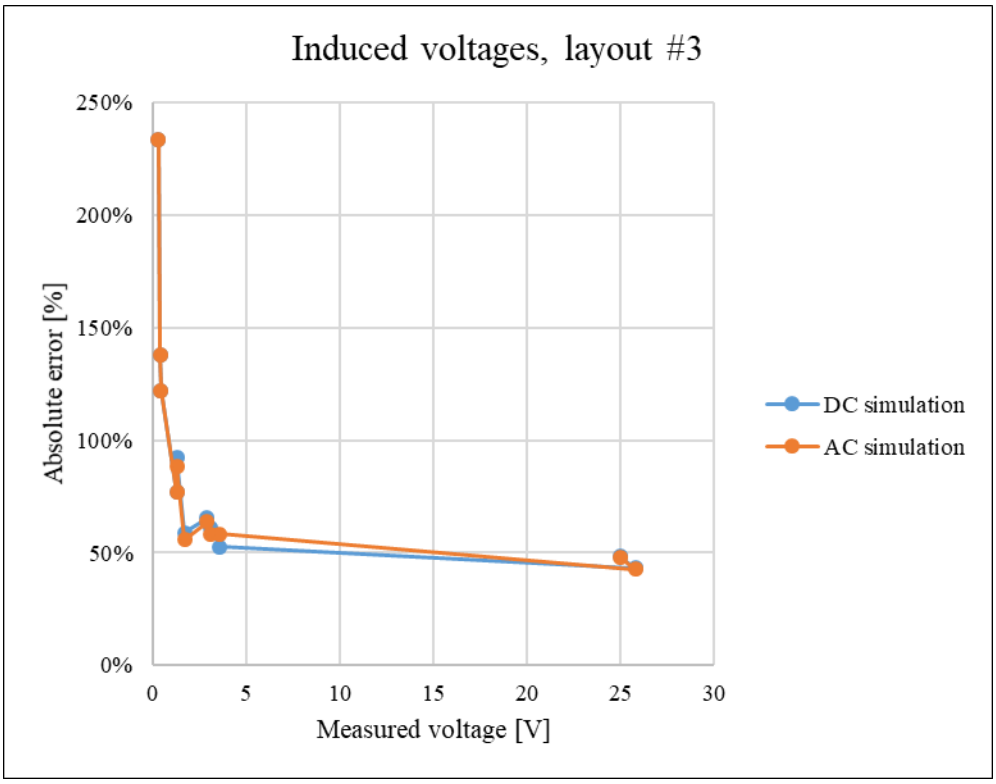


Figure 8-5: Induced voltage estimation error, layout #3

9 Summary

In this diploma thesis, I overviewed some possible parasitic analysis methods, which can be used during the design process of power electronic systems. I tested the methods learned on three different half-bridge circuits designed by myself. My goal was to compare the methods tried, and choose the most appropriate one(s), if it is possible. Finally, I can say, that this project was successful, because this goal is completed.

According to Chapter 8.2, it can be said that the parasitic analysis based on finite element analysis is a proper method for investigating layout related parasitic effects. The Q3D Extractor software module of ANSYS Electromagnetics is appropriate to execute the FEA. I got valuable experiences with this software, which will be useful in future projects. With this method, I can model the parasitic effects of the three different layouts such that the simulated characteristics converge to the measured ones. With this method, an upper limit can be provided to the peak values of the induced voltages.

Besides I proved the competency of the FEM, I highlighted that the parasitic analysis based on rules of thumb, and analytical approximations – that are often used methods – are not proper, and their usage should be avoided.

With this project, I got experience in measurements, too. An important result is that the estimation of inductance of conductive paths is possible through indirect measurements (see in Chapter 7.2).

As I mentioned in the Introduction, nothing can be completely exact in this area of electronics. The results concerning layout #3 prove this statement. One of my future goals is to refine the parasitic model of this circuit, and reach higher accuracy in the observed parameters. Another goal is to get more experience with the Q3D Extractor software module through investigating the more sophisticated functions of it.

Acknowledgements

I am grateful to György Orosz, my internal advisor at the university, who supported my project works through three years.

I would like to thank András Mersich, my external consultant at Robert Bosch Ltd. for all his guidance and assistance through my work.

I am also grateful to my colleagues, Marcell Horváth and Zsolt Sükösd for their patience and useful advices given, and to Gábor Vadócz for the support in creating the geometry models of the circuits.

I would like to thank to Robert Bosch Ltd. for financing my project and providing me the opportunity and the equipment to complete this diploma thesis.

Bibliography

[1] Wikipedia. (January 21, 2018). Retrieved May 17, 2018, from Bridge circuit: https://en.wikipedia.org/wiki/Bridge_circuit

[2] Wikipedia. (April 9, 2018). Retrieved May 17, 2018, from H bridge: https://en.wikipedia.org/wiki/H_bridge

[3] Wikipedia. (May 7, 2018). Retrieved May 17, 2018 from Finite element method: https://en.wikipedia.org/wiki/Finite_element_method

[4] ON Semiconductor. (February 2016). Retrieved May 17, 2018, from: NCP5111 High Voltage, High and Low Side Driver. https://www.onsemi.com/pub/Collateral/NCP5111-D.PDF

[5] Infineon. (July 2012). Retrieved May 17, 2018, from: OptiMOS-T2 Power-Transistor. https://www.infineon.com/dgdl/Infineon-IPP_B_I100N04S4_H2-DS-v01_00-en.pdf?fileId=db3a304328c6bd5c01291c2758925d17

[6] Multicomp. (July 2011). Retrieved May 17, 2018 from: General Purpose Capacitors, MCRH Series. http://www.farnell.com/datasheets/2570357.pdf

[7] Paul, Clayton R. (2009) Inductance: Loop and Partial. Hoboken, NY: John Wiley & Sons.

[8] Gábor Grabicza: Impedance Analysis with Agilent E5061B Network Analyzer. BSc thesis, 2015.

[9] PEM (Power Electronic Measurement). (August 2013). Retrieved May, 2018 from: CWT Ultra-mini.

http://www.pemuk.com/Userfiles/CWTum%2030MHz/CWT%20Ultra-mini_0318.pdf

[10] Fairchild. (December 2014). Retrieved May 17, 2018 from: Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC. https://www.fairchildsemi.com/application-notes/AN/AN-6076.pdf

[11] Infineon. (March 2012). Retrieved May 17, 2018 from: Infineon OptiMOS Power MOSFET Datasheet Explanation.

https://www.infineon.com/dgdl/Infineon-MOSFET_OptiMOS_datasheet_explanation-AN-v01_00-EN.pdf?fileId=db3a30433b47825b013b6b8c6a3424c4

[12] IXYS. (June 2013). Retrieved May 17, 2018 from: IX2127 Design Considerations.

http://www.ixysic.com/home/pdfs.nsf/www/AN-400.pdf/$file/AN-400.pdf

[13] Dodge, Jonathan. (March, 2006). Retrieved May 17, 2018 from: Power MOSFET Tutorial.

https://www.microsemi.com/document-portal/doc_view/14692-mosfet-tutorial

[14] Nexperia. (February 2014). Retrieved May 17, 2018 from: Understanding Power MOSFET Data Sheet Parameters.

https://assets.nexperia.com/documents/application-note/AN11158.pdf

[15] International Rectifier, Vrej Barkhordarian. Retrieved May 17, 2018 from: Power MOSFET basics.

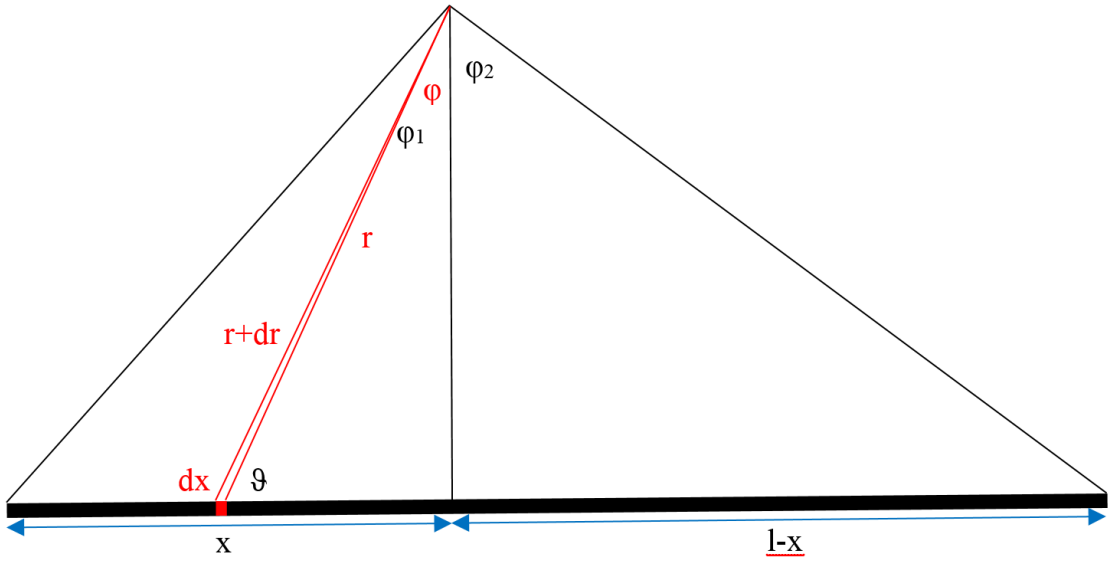
https://www.infineon.com/dgdl/an-1084.pdf?fileId=5546d462533600a401535595840d101e

[16] Fodor, György. (1999). Elektromágneses terek. Budapest: Műegyetemi Kiadó.

Appendix

Inductance of a finite length cylindrical wire

External inductance



Biot-Savart's law:

$$d\vec{B} = \frac{\mu_0 I}{4\pi} \cdot \frac{d\vec{l} \times \vec{r}}{r^3}$$

$$dB_{ext} = \frac{\mu_0 I}{4\pi} \cdot \frac{sin\vartheta}{r^2} \cdot dl$$

$$dl \cdot sin\vartheta \cong r \cdot d\varphi$$

$$cos\varphi = \frac{y}{r}$$

$$dB_{ext} = \frac{\mu_0 I}{4\pi} \cdot \frac{r \cdot d\varphi}{r^2} = \frac{\mu_0 I}{4\pi} \cdot \frac{d\varphi}{r} = \frac{\mu_0 I}{4\pi} \cdot \frac{cos\varphi \, d\varphi}{y} = \frac{\mu_0 I}{4\pi y} \cdot cos\varphi \, d\varphi$$

$$B_{ext} = \int_{-\varphi_1}^{\varphi_2} dB_{ext} = \int_{-\varphi_1}^{\varphi_2} \frac{\mu_0 I}{4\pi y} \cdot cos\varphi \, d\varphi = \frac{\mu_0 I}{4\pi y} \cdot \int_{-\varphi_1}^{\varphi_2} cos\varphi \, d\varphi = \frac{\mu_0 I}{4\pi y} \cdot [sin\varphi]_{-\varphi_1}^{\varphi_2}$$

$$B_{ext}(y) = \frac{\mu_0 I}{4\pi y} \cdot (sin\varphi_1 + sin\varphi_2)$$

$$sin\varphi_1 = \frac{x}{\sqrt{x^2 + y^2}}$$

$$sin\varphi_2 = \frac{l-x}{\sqrt{(l-x)^2+y^2}}$$

$$B_{ext}(x,y) = \frac{\mu_0 I}{4\pi y} \cdot \left(\frac{x}{\sqrt{x^2+y^2}} + \frac{l-x}{\sqrt{(l-x)^2+y^2}} \right)$$

$$\Phi_{ext} = \int_R^{\infty} \int_0^{l} B(x,y)\, dx\, dy = \frac{\mu_0 I}{4\pi} \cdot \int_0^{\infty} \frac{1}{y} \cdot \int_0^{l} \left(\frac{x}{\sqrt{x^2+y^2}} + \frac{l-x}{\sqrt{(l-x)^2+y^2}} \right) dx\, dy$$

$$\int f^n \cdot f' = \frac{f^{n+1}}{n+1}$$

$$\int_0^{l} \left(\frac{x}{\sqrt{x^2+y^2}} + \frac{l-x}{\sqrt{(l-x)^2+y^2}} \right) dx = \int_0^{l} \frac{x}{\sqrt{x^2+y^2}} dx + \int_0^{l} \frac{l-x}{\sqrt{(l-x)^2+y^2}} dx =$$

$$= \frac{1}{2} \cdot \int_0^{l} \frac{2x}{\sqrt{x^2+y^2}} dx - \frac{1}{2} \cdot \int_0^{l} \frac{2(l-x)\cdot(-1)}{\sqrt{(l-x)^2+y^2}} dx =$$

$$= \left[\sqrt{x^2+y^2} \right]_0^{l} - \left[\sqrt{(l-x)^2+y^2} \right]_0^{l} = \sqrt{l^2+y^2} - y - y + \sqrt{l^2+y^2} =$$

$$= 2 \cdot \left(\sqrt{l^2+y^2} - y \right)$$

$$\Phi_{ext} = \frac{\mu_0 I}{4\pi} \cdot \int_0^{\infty} \frac{1}{y} \cdot 2 \cdot \left(\sqrt{l^2+y^2} - y \right) dy = \frac{\mu_0 I}{2\pi} \cdot \int_0^{\infty} \left(\frac{\sqrt{l^2+y^2}}{y} - 1 \right) dy =$$

$$= \frac{\mu_0 I}{2\pi} \cdot \left[\sqrt{l^2+y^2} - l \cdot ln\left(l \cdot \left(\sqrt{l^2+y^2} + l \right) \right) + l \cdot lny - y \right]_R^{\infty} =$$

$$= \frac{\mu_0 I}{2\pi} \cdot \left[\sqrt{l^2+y^2} - y - l \cdot \left(lnl + \ln \frac{\sqrt{l^2+y^2}+l}{y} \right) \right]_R^{\infty} =$$

$$= \frac{\mu_0 I}{2\pi} \cdot \lim_{y\to\infty} \left(\sqrt{l^2+y^2} - y - l \cdot \left(lnl + \ln \frac{\sqrt{l^2+y^2}+l}{y} \right) \right) -$$

$$- \frac{\mu_0 I}{2\pi} \cdot \left(\sqrt{l^2+R^2} - R - l \cdot \left(lnl + \ln \frac{\sqrt{l^2+R^2}+l}{R} \right) \right)$$

Assumption:

$$l \gg R$$

$$\Phi_{ext} = \frac{\mu_0 I}{2\pi} \cdot \left(\lim_{y\to\infty} \left(\sqrt{l^2 + y^2} - y \right) - l \cdot lnl - l \cdot \lim_{y\to\infty} \ln \frac{\sqrt{l^2 + y^2} + l}{y} \right) -$$

$$- \frac{\mu_0 I}{2\pi} \cdot \left(\sqrt{l^2 + R^2} - R - l \cdot \left(lnl + \ln \frac{\sqrt{l^2 + R^2} + l}{R} \right) \right) \cong$$

$$\cong \frac{\mu_0 I}{2\pi} \cdot (0 - l \cdot lnl - l \cdot ln1) - \frac{\mu_0 I}{2\pi} \cdot \left(l - R - l \cdot lnl - l \cdot \ln \frac{2l}{R} \right) =$$

$$= \frac{\mu_0 I}{2\pi} \cdot \left(-l \cdot lnl - l + R + l \cdot lnl + l \cdot \ln \frac{2l}{R} \right) \cong$$

$$\cong \frac{\mu_0 I}{2\pi} \cdot l \cdot \left(\ln \frac{2l}{R} - 1 \right)$$

$$L_{ext} = \frac{\Phi_{ext}}{I} = \frac{\mu_0}{2\pi} \cdot l \cdot \left(ln \frac{2l}{R} - 1 \right)$$

Internal inductance

Maxwell I. (Ampére's law):

$$\oint_L \vec{H}\, d\vec{l} = \int_A \vec{J}\, d\vec{A}$$

The magnetic field inside the wire:

$$H(r) \cdot 2r\pi = I \cdot \frac{r^2 \pi}{R^2 \pi}$$

$$H(r) = \frac{I \cdot r}{2R^2 \pi}$$

The energy of the magnetic field:

$$\int_V \frac{1}{2} \cdot \mu_0 \cdot H^2 dV = \frac{1}{2} \cdot L_{int} \cdot I^2$$

$$L_{int} = \frac{\mu_0}{I^2} \cdot \int_V H^2 dV$$

The volume integral with spherical coordinates:

$$L_{int} = \frac{\mu_0}{I^2} \cdot l \cdot \int_0^R \left(\frac{I \cdot r}{2R^2\pi}\right)^2 \cdot 2r\pi \, dr = \frac{\mu_0}{I^2} \cdot l \cdot \int_0^R \frac{I^2 \, r^2}{4R^4\pi^2} \cdot 2r\pi \, dr =$$

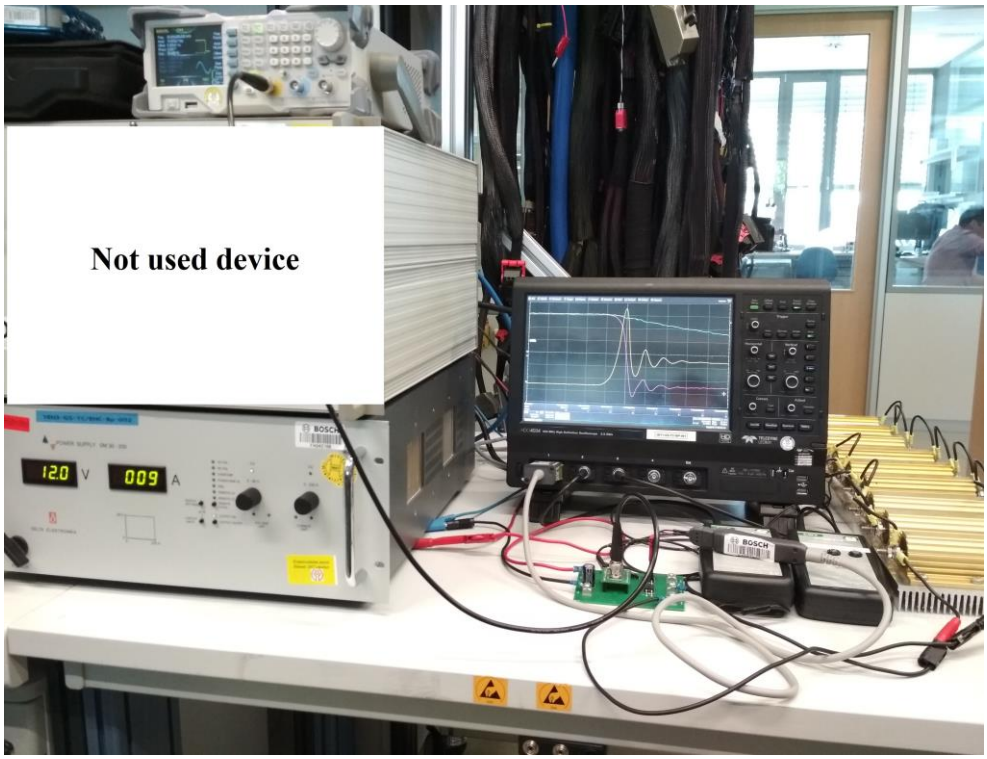
$$= \frac{\mu_0}{2R^4\pi} \cdot l \cdot \int_0^R r^3 dr = \frac{\mu_0 l}{8\pi}$$

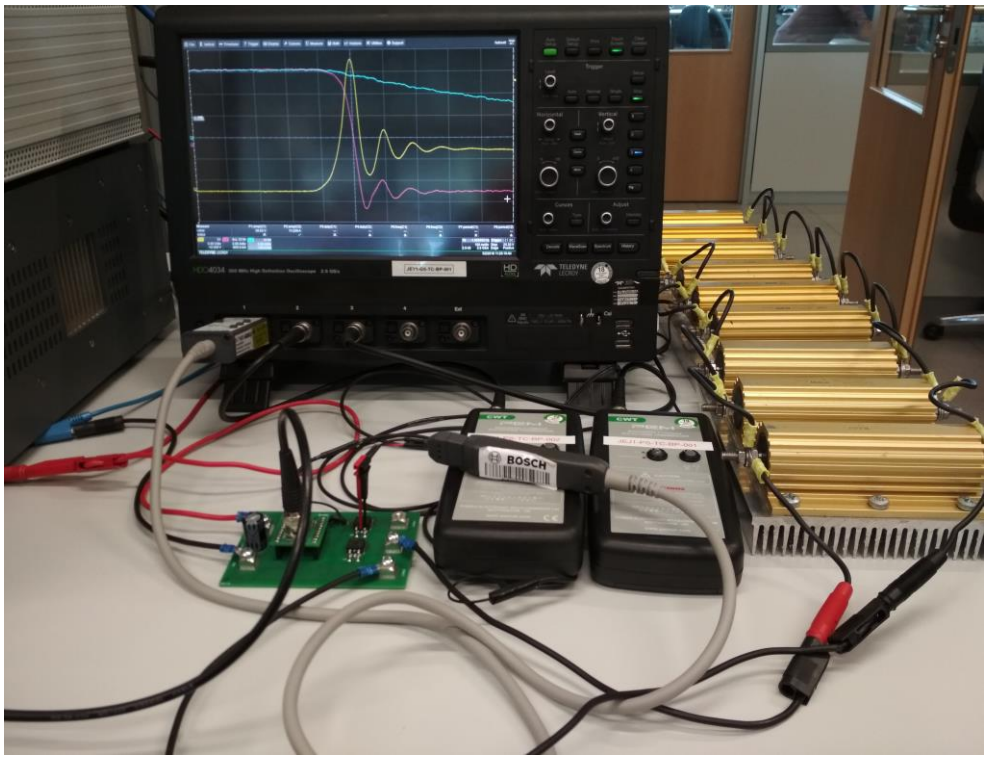
Total inductance

$$L = L_{ext} + L_{int} = \frac{\mu_0}{2\pi} \cdot l \cdot \left(ln\frac{2l}{R} - 1\right) + \frac{\mu_0 l}{8\pi} = \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln\frac{2l}{R} - 1 + \frac{1}{4}\right)$$

$$L = \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln\frac{2l}{R} - 0.75\right) \equiv \frac{\mu_0}{2\pi} \cdot l \cdot \left(\ln\frac{4l}{d} - 0.75\right)$$

Measurement setup

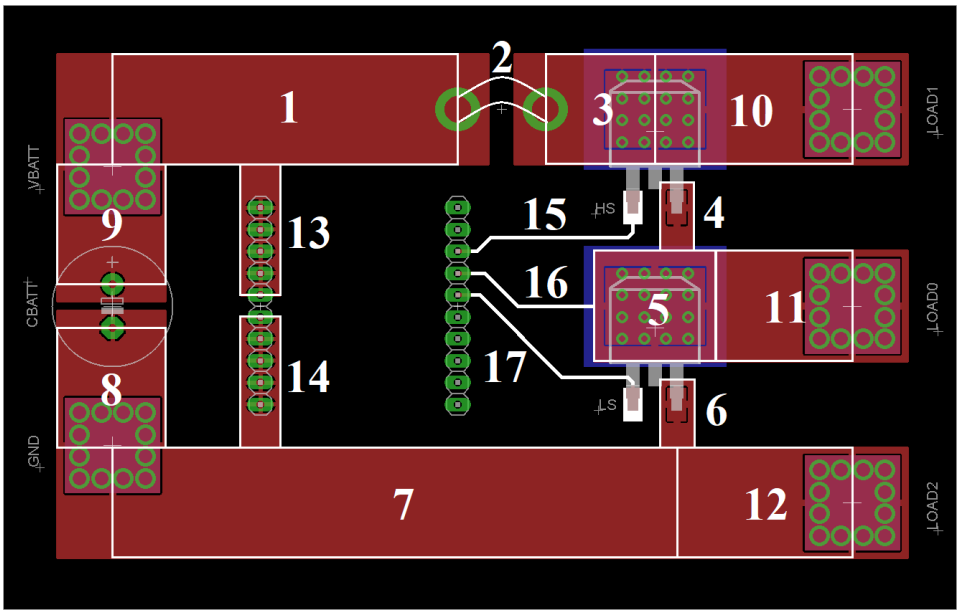




Parasitic analysis

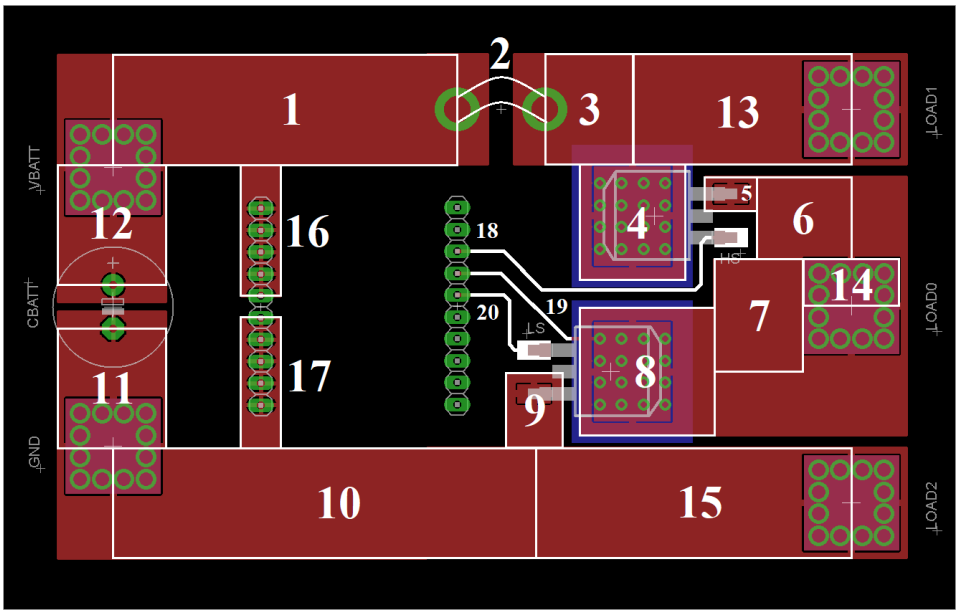
Rectangular-shaped segmentation and parameters

Layout #1



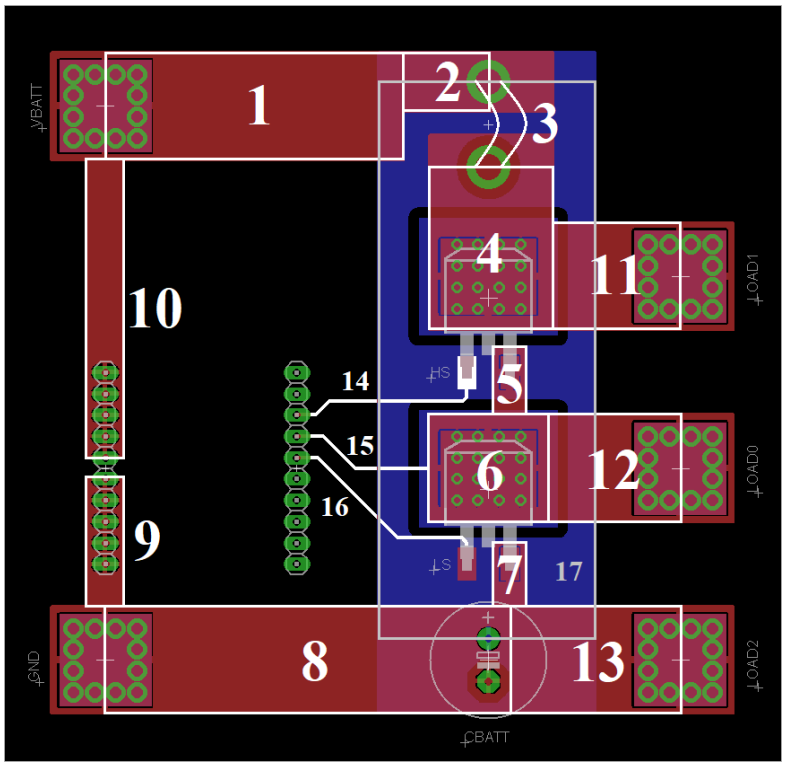
Segment	Length$_{mm}$	Width$_{mm}$	Rule o.t$_{nH}$	DCL$_{nH}$	DCR$_{m\Omega}$
1	40	13	40	19	3.0
2	32	3.25	32	19	0.1
3	13	13	13	4	1.0
4	8	3.75	8	3	2.1
5	13	15	13	4	0.8
6	8	3.75	8	3	2.1
7	66	13	66	38	4.9
8	14	13	14	4	1.0
9	14	13	14	4	1.0
10	23	13	23	9	1.7
11	16	13	16	5	1.2
12	21	13	21	8	1.6
13	15	5	15	7	2.9
14	15	5	15	7	2.9
15	22	0.41	22	23	52.3
16	16	0.41	16	16	38.0
17	25	0.41	25	27	59.4

Layout #2



Segment	Length$_{mm}$	Width$_{mm}$	Rule o.t$_{nH}$	DCL$_{nH}$	DCR$_{m\Omega}$
1	40	13	40	19	3.0
2	32	3.25	32	19	0.1
3	10	13	10	3	0.7
4	16	13	16	5	1.2
5	8	3.75	8	3	2.1
6	15	8	15	6	1.8
7	20	17	20	7	1.1
8	20	18	20	6	1.1
9	12	8	12	4	1.5
10	49	13	49	26	3.7
11	14	13	14	4	1.0
12	14	13	14	4	1.0
13	30	13	30	13	2.2
14	4	13	4	1	0.3
15	38	13	38	18	2.8
16	15	5	15	7	2.9
17	15	5	15	7	2.9
18	35	0.41	35	40	83.2
19	16	0.41	16	16	38.0
20	13	0.41	13	12	30.9

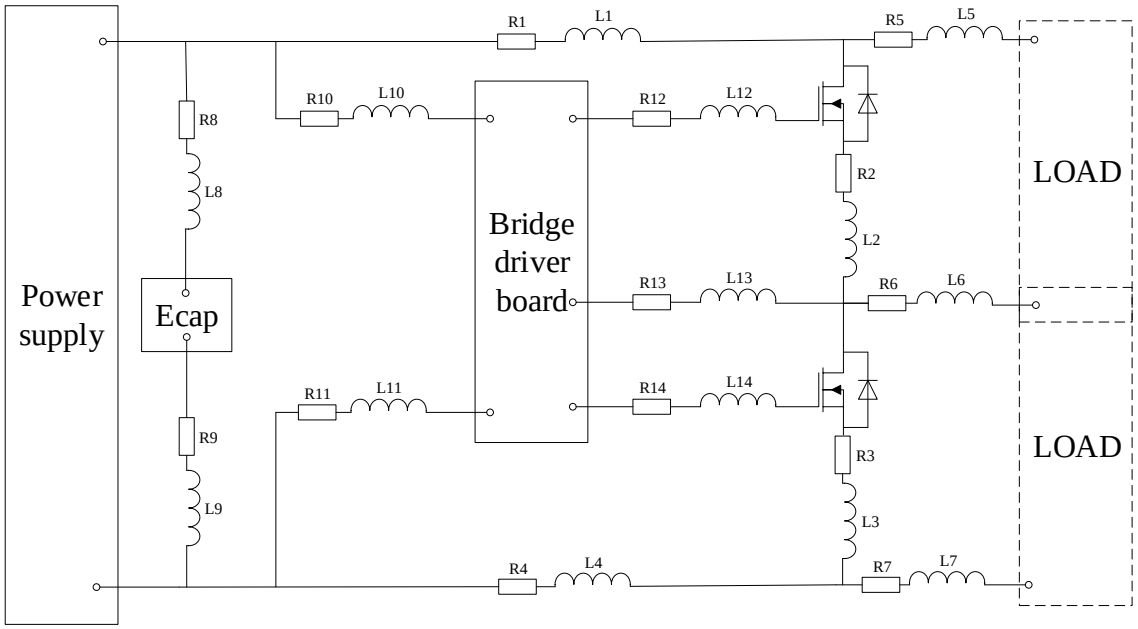
Layout #3



Segment	Length$_{mm}$	Width$_{mm}$	Rule o.t$_{nH}$	DCL$_{nH}$	DCR$_{m\Omega}$
1	33	13	33	15	2.5
2	5	7.5	5	1	0.6
3	32	3.25	32	19	0.1
4	20	15	20	7	1.3
5	8	3.75	8	3	2.1
6	13	15	13	4	0.8
7	8	3.75	8	3	2.1
8	40	13	40	19	3.0
9	15	5	15	7	2.9
10	36	5	36	23	7.0
11	16	13	16	5	1.2
12	15	13	15	5	1.1
13	22	13	22	8	1.6
14	22	0.41	22	23	52.3
15	16	0.41	16	16	38.0
16	25	0.41	25	27	59.4
17	80	26	80	39	3.0

Parasitic models

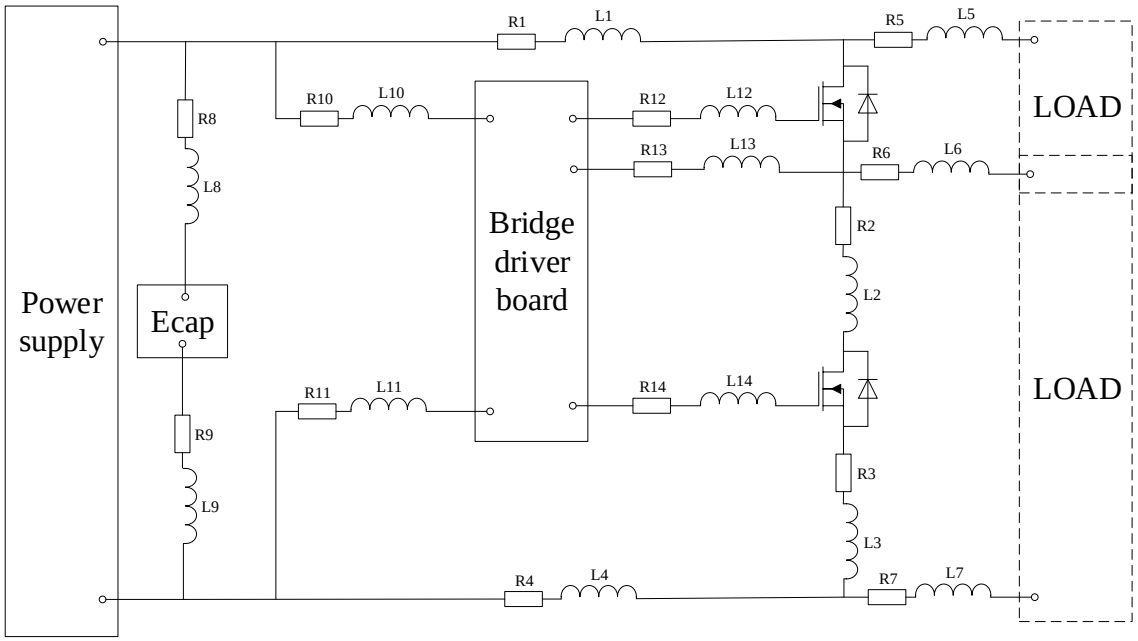
Layout #1



Parameters:

#	DCR with formula	DCL with rule of thumb	DCL with formula	DCL with simulation	DCR with simulation	ACL with simulation @ 20 kHz	ACR with simulation @ 20 kHz
1	4	85	42	35	3.5	32	3.8
2	3	21	7	2	1.1	2	1.1
3	2.1	8	3	3	1.4	3	1.4
4	4.9	66	38	35	4.6	33	4.8
5	1.7	23	9	4	0.9	3	1
6	1.2	16	5	8	2.2	7	2.3
7	1.7	23	9	5	1.1	4	1.2
8	1	14	4	3	0.9	2	0.9
9	1	14	4	3	0.9	2	0.9
10	2.9	15	7	5	2.2	5	2.2
11	2.9	15	7	5	2.2	5	2.2
12	52.3	22	23	22	50	22	50
13	38	16	16	20	44.3	20	44.8
14	59.4	25	27	30	71.5	30	72

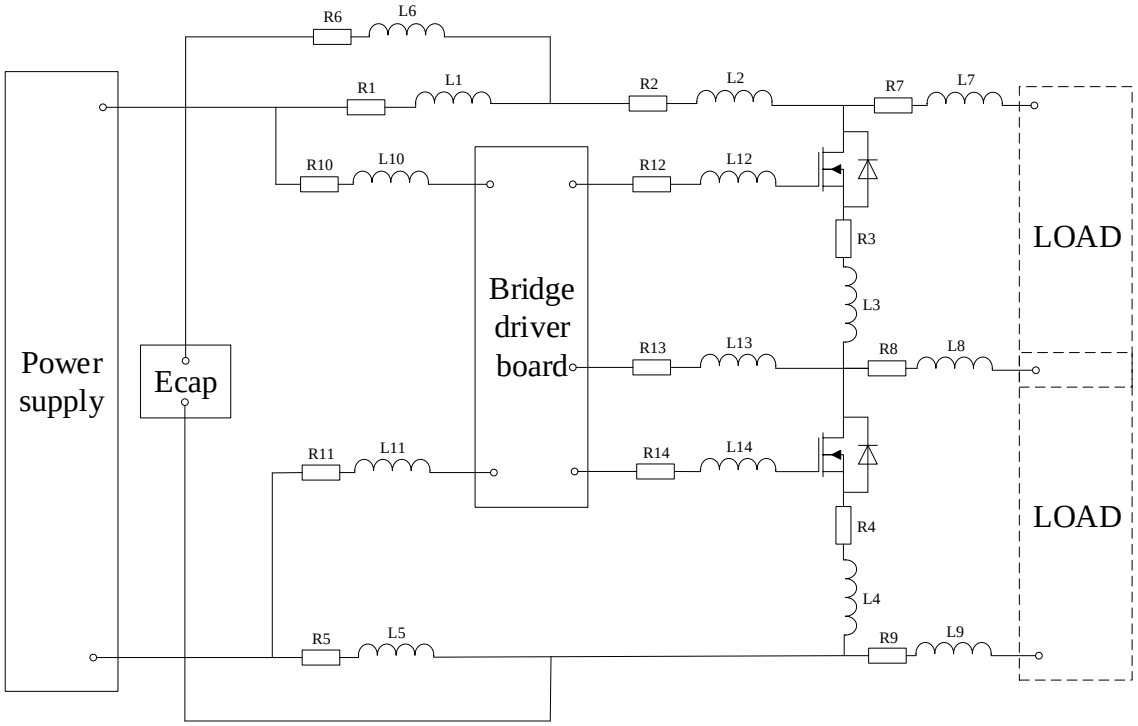
Layout #2



Parameters:

#	DCR with formula	DCL with rule of thumb	DCL with formula	DCL with simulation	DCR with simulation	ACL with simulation @ 20 kHz	ACR with simulation @ 20 kHz
1	5	98	46	36	3.7	32	4
2	6.1	63	22	12	2.8	11	3
3	1.5	12	4	4	1.4	4	1.5
4	3.7	49	26	23	3.4	21	3.5
5	2.2	30	13	9	1.7	7	1.8
6	0.3	4	1	5	1.6	4	1.7
7	2.8	38	18	14	2.4	12	2.5
8	1	14	4	3	0.9	2	0.9
9	1	14	4	3	0.9	2	0.9
10	2.9	15	7	5	2.2	5	2.2
11	2.9	15	7	4	2.2	6	2.4
12	83.2	35	40	38	85.4	38	85.4
13	38.0	16	16	19	43	19	43.1
14	30.9	13	12	10	26.7	10	26.7

Layout #3

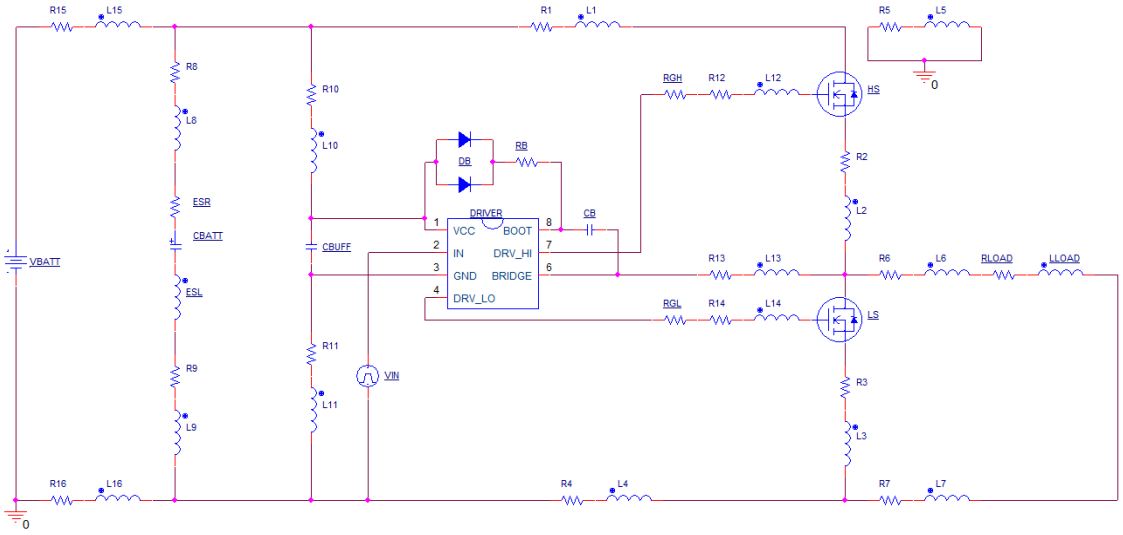


Parameters:

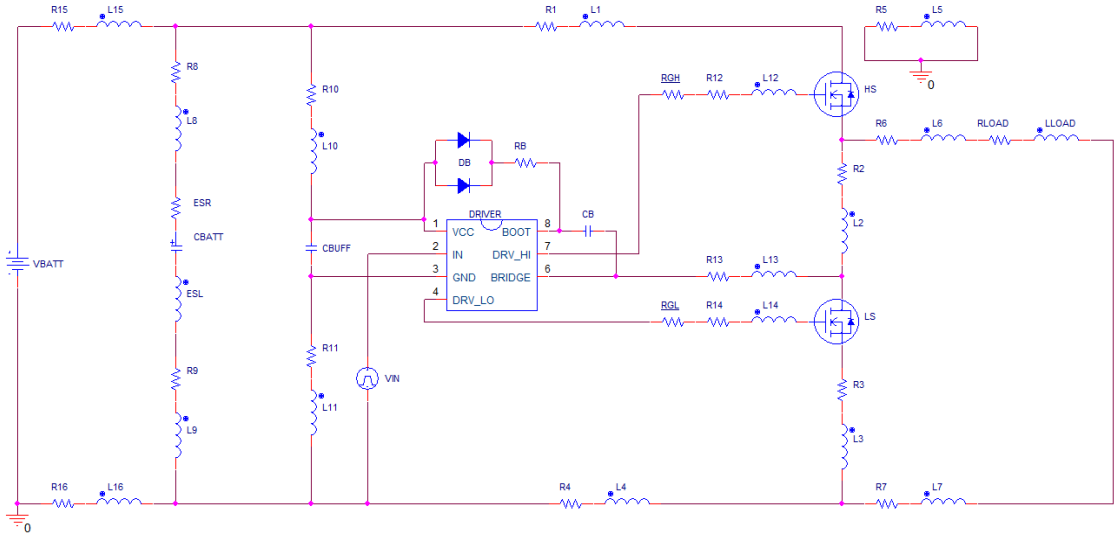
#	DCR with formula	DCL with rule of thumb	DCL with formula	DCL with simulation	DCR with simulation	ACL with simulation @ 20 kHz	ACR with simulation @ 20 kHz
1	3.1	38	16	21	3.6	20	3.8
2	1.4	52	26	12	0.8	11	0.9
3	2.9	21	7	2	1.1	2	1.1
4	2.1	8	3	5	1.9	5	1.9
5	3	40	19	21	3.3	20	3.4
6	3	80	39	35	7.8	35	7.8
7	1.2	16	5	4	0.9	3	1
8	1.1	15	5	8	2.3	7	2.3
9	1.6	22	8	7	1.6	6	1.7
10	7	36	23	23	7.1	23	7.2
11	2.9	15	7	7	2.9	7	3
12	52.3	22	23	21	48.3	21	48.3
13	38	16	16	19	41.9	19	41.9
14	59.4	25	27	26	58.7	26	58.7

Electrical simulation models

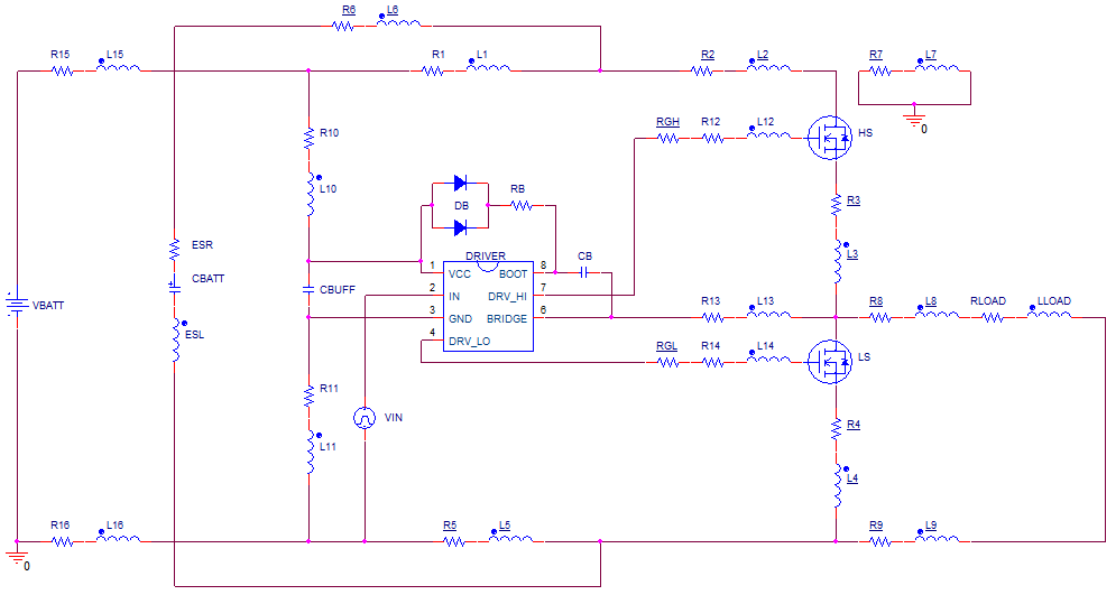
Layout #1



Layout #2



Layout #3


R6
L6
R15
L15
R1
L1
R2
L2
R7
L7
RGH
R12
L12
HS
R10
L10
DB
RB
R3
ESR
CBATT
DRIVER
CB
L3
VBATT
CBUFF
VCC
BOOT
IN
DRV_HI
GND
BRIDGE
DRV_LO
R13
L13
R8
L8
RLOAD
LLOAD
RGL
R14
L14
LS
ESL
R11
VIN
R4
L11
L4
R16
L16
R5
L5
R9
L9
0

Measurement results

Layout #1

Load	Contact points		Measured [V]	DC simulation [V]	AC simulation [V]
LS	LSD	HSS	0.53	1	1
HS	GND	LSS	5.4	8.2	8.3
HS	HSD	VBATT	7.2	10.9	11.1
LS	HSD	VBATT	9	13.3	13.8
LS	GND	LSS	9.2	13.6	13.9
HS	HSD	HSS	25	34	33.5
LS	LSD	LSS	36	44.4	43.9

Layout #2

Load	Contact points		Measured [V]	DC simulation [V]	AC simulation [V]
HS	HSS	LSD	0.52	1	1
LS	GND	LSS	2.1	3.2	3.3
HS	GND	LSS	3.2	5.1	5
HS	HSD	VBATT	4.1	6	6.1
LS	HSD	VBATT	7.1	10	9.7
HS	LSD	LSS	27	34.5	34
LS	HSD	HSS	31.1	38.4	38.2

Layout #3

Load	Contact points		Measured [V]	DC simulation [V]	AC simulation [V]
HS	ECAP-	LSS	0.3	1	1
HS	LSD	HSS	0.42	1	1
LS	LSD	HSS	0.45	1	1
HS	WIRE+	VBATT	1.3	2.3	2.3
HS	HSD	WIRE+	1.3	2.5	2.45
LS	WIRE+	VBATT	1.7	2.7	2.65
LS	WIRE+	ECAP+	2.9	4.8	4.75
HS	WIRE+	ECAP+	3.1	5	4.9
LS	HSD	WIRE+	3.6	5.5	5.7
LS	HSD	HSS	25.8	37	36.8
HS	LSD	LSS	25	37.1	37