Abstract

This master thesis presents the details of the design and implementation of the firmware of an intelligent camera system, the so called EDICAM (Event Detection Intelligent Camera). The firmware has been implemented on two FPGAs.

The EDICAM system consists of a camera head and a development board. These hardware modules have already been available at the beginning of the development. The first part of the thesis presents some details of these hardware components as well as introduces the third party FPGA modules. These modules are responsible to handle the low level interfaces connected to the FPGAs. Firmware design on FPGAs requires specific timing considerations which are introduced as well.

The development of the firmware was based on the high level specification of EDICAM, so the second part of the thesis is focused on certain parts of this document: exposure and image readout methodology of EDICAM.

The introduction of the specification is followed by the details of the system level design. This part presents the high level architecture of the two main firmware components, and shortly introduces the submodules and the main interfaces. The submodules which are the main contributions of my development are introduced in detail in the next part one-by-one.

The last part of the thesis demonstrates and summarizes the operation of EDICAM via presenting test results: 2 exposures and a transmission of an image had been performed.

In summary, it can be said that the inital objectives have been completely achieved. The implementation introduced in this thesis complies with the high level specification of EDICAM.