

# Abstract

Parasitic analysis has a significant role in designing power electronics systems. The analysis does not only contain the derivation of parasitic effects related to the manufacturing technology of components, but also the layout related parameters. The collection of these parasitic effects fundamentally determine the power dissipation – that is linked with the parasitic resistance – and the switching processes of the circuits.

The switching losses can be reduced by reducing the switching times, but the reduction is limited by the parasitic inductances appearing in the system. The induced voltage spikes appearing in the moments of switching due to them are not allowed to exceed the critical characteristic values of the components, otherwise component damage is imminent. When breaking high currents in power electronics circuits, the induction caused by the parasitic effects always has to be considered.

In this diploma thesis, as part of a design process, I overview the applicable methods for parasitic analysis. I focus on the layout related parasitic effects. I also focused on getting experience in use of ANSYS Q3D Extractor finite element software, because according to my assessment, it provides the most realistic modelling of parasitic effects.

I introduce the methods through the example of a classic half-bridge topology. This circuit is simple to design, but is also representative, because a typical switching procedure can be observed through it. The half-bridge circuit is realized with three different topologies, on printed circuit boards.

Finally, I compared the results of parasitic analysis based on different methods with the behavior of real operation. The output of my work is a methodology of parasitic analysis based on finite element field simulation, that can be used in future projects.